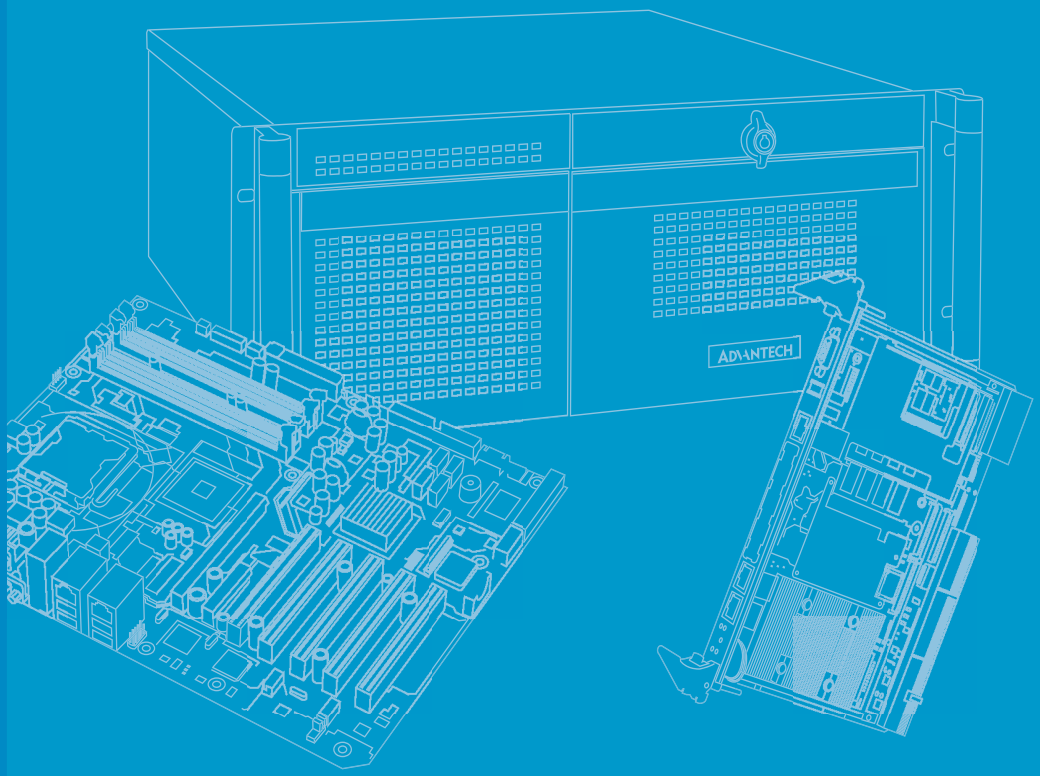

User Manual

ITA-2210

2U Fanless Rackmount Embedded Industrial Computer based on a Intel® Atom™ Dual-Core Processor

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgements

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For technical support and service, please visit our support website at:

http://support.advantech.com

Part No. 200K221030 Edition 1

Printed in China September 2014

Product Warranty (2 years)

Advantech warrants the original purchaser that all its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, customers are billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product is defective, please follow the steps listed below:

1. Collect all information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any relevant information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and proof of purchase date (such as a photocopy of your sales receipt) in a shippable container. Products returned without proof of the purchase date are not eligible for our warranty service.
5. Write the RMA number clearly on the outside of the package and ship the product prepaid to your dealer.

A Message to the Customer

Advantech Customer Services

Every Advantech product is built with the most exact specifications to ensure reliable performance in the harsh and demanding conditions typical of industrial environments. Whether your new Advantech product is destined for a laboratory or factory floor, you can be assured that your product will deliver the reliability and ease-of-operation for which the name Advantech is renowned. Your satisfaction is our primary concern. The following information is intended to provide a guide to Advantech's customer services.

To ensure you receive the full benefit of our services, please follow the instructions provided below.

Technical Support

We want you to experience the best performance possible from your products. Should you encounter technical difficulties, we are available to provide assistance. The answers to the most frequently asked questions are provided in the product documentation. These answers are typically a lot more detailed than the ones provided over the phone.

Please consult this manual first. If you still cannot find the answer, gather all information or questions that apply to your problem, and with the product in hand, call your dealer. Our dealers are well trained and ready to provide the support you need to get the most from your Advantech products. However, most of the problems reported are minor and can be easily solved over the phone.

In addition, free technical support from Advantech engineers is available every business day. We are always ready to give advice about application requirements or specific information regarding the installation and operation of any of our products.

Initial Inspection

Upon opening the shipping carton, please ensure that the following items have been shipped:

- ITA-2210 series industrial computer
- ITA-2210 accessory box
- Warranty card

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We careful inspect all ITA-2210 systems both mechanically and electrically before shipment. Thus, the product should be free of marks and scratches and in perfect working order upon receipt. When unpacking ITA-2210, check the unit for signs of shipping damage (for example, packaging damage, scratches, dents, etc.). If the product is damaged or fails to meet the specifications, please notify our service department or your local sales representative immediately. Also, please notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect this equipment from all AC outlets before cleaning. Use only a damp cloth for cleaning. Do not apply liquid or spray detergents.
4. For plugged-in equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect this equipment from humidity.
6. Place this equipment on a reliable surface during installation. Dropping or letting the device fall may cause damage.
7. Ensure the power source voltage is correct before connecting the equipment to a power outlet.
8. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
9. All cautions and warnings on the equipment should be noted.
10. If unused for a lengthy period, disconnect the equipment from the power source to avoid damage from transient overvoltage.
11. Never pour liquids into an opening. This may cause fire or electrical shock.
12. Never open the equipment. For safety reasons, the equipment should only be opened by qualified service personnel.
13. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
14. Do not store this equipment in an environment with a room temperature of below -25 °C (13 °F) or above 60 °C (140 °F); this can damage the equipment.
15. This equipment has been tested and found to comply with the specifications for a Class-A digital device. Operation of this equipment in a residential area is likely to cause harmful interference, in which case, users are required to correct this interference at their own expense.
16. Advantech does not provide a power component for this product. Users are advised to purchase power components with CCC certification.
17. CAUTION: The computer is equipped with a battery-powered real-time clock circuit. Thus, an explosion may occur if the battery is incorrectly replaced. Replace the provided battery with only the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
18. The sound pressure level at the operator position should not exceed 70 dB (A), according to IEC 704-1:1982.

DISCLAIMER: These instructions are provided according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precautions - Static Electricity

Follow the simple precautions listed below to protect yourself from harm and the products from damage:

1. To avoid electrical shock, always disconnect the power from your PC chassis before manually handling the device. Do not touch any components on the CPU card or other cards when the PC is powered on.
2. Disconnect the power before implementing configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Contents

Chapter 1

Overview

This chapter provides general information about the ITA-2210 system.

- Introduction
- Specifications
- Power Information
- Environmental Specifications
- Dimensions

1.1 Introduction

The ITA-2210 is a 2U fanless rackmount embedded industrial computer equipped with an Intel® Atom™ dual-core processor and wide voltage input range. This powerful computing platform provides an integrated management system for surveillance and communication that can withstand 24-7 operation.

1.2 Specifications

- **Processor and Chipset:** Intel® Atom™ processor 525 + Intel® ICH 8 M chipset
- **BIOS:** AMI SPI 16-Mb Flash
- **Memory:** 2 GB DDR3 800 onboard
- **Display:** Embedded Gen3.5+GFX core, 400 MHz frequency
- **Dual Display:**
  - Single-display resolution of up to 2048 x 1536 @ 60 Hz
  - Dual-display resolution of up to 1366x 768 @ 60 Hz
- **Storage:** Supports one CF slot and one 3.5" or two 2.5" HDD slots
- **Expansion Slot:** Supports three ITAM slots, one PC104+ interface, and one Mini PCIe slot
- **Ethernet:** Two 10/100/1000M Ethernet RJ45 connectors
- **USB:** Eight USB 2.0 ports
- **VGA:** Two VGA ports
- **Serial Ports:** Two DB9 ports, RS-232/422/485 switchable
- **Digital I/O:** One eight-channel TTL GPIO
- **Audio:** One speaker output with 2 x 4 W amplifiers, and one mic-in jack
- **Reserved Zone (with optional rear panel):** One PCI 104 interface
- **ITAM I/O Module (optional):**
  - ITAM-SR01-10A1E supports eight serial ports (RS-232/422/485)
  - ITAM-SR01-00A1E supports eight serial ports (RS-232/422/485) with 2.5 KV photo coupler isolation
  - ITAM-NC01-C0A1E supports eight 10/100/1000M Ethernet RJ45 connectors
  - ITAM-NC02-C0A1E supports four 10/100/1000M Ethernet RJ45 connectors
  - ITAM-NC02-F0A1E supports four 10/100/1000M SFP connectors
- **Dimensions (W x H x D):** 483 x 88 x 325 mm
- **Net Weight:**
  - - Single Power: 7.7 kg
  - - Dual Power: 8 kg

1.3 Power Information

ITA-2210 supports a hot-swappable power supply module. Uses can choose either dual power or single power depending on their requirements.

Table 1.1: Power Supply

DC / AC Voltage Input	110 V_{DC} / 100-240 V_{AC}
Current Input	110 V_{DC} - 0.82 A 100 - 240 V_{AC} - 1.08 A ~ 0.45 A
Power Input Connector	3P terminal block (European standard)

1.4 Environmental Specifications

Table 1.2: Environmental Specifications	
Operating Temperature	With HDD: 0 ~ 40 °C
	With SSD: -25 ~ 60 °C (With 0.7 m/s airflow)
Storage Temperature	-40 ~ 85 °C
Humidity	95% @ 40 °C, non-condensing
Vibration	With 2.5" SSD: 2 Grms @ 5 ~ 500 Hz, random, 1 hr/axis.
	With 2.5" HDD: 1 Grms @ 5 ~ 500 Hz, random, 1 hr/axis.
	IEC60068-2-6 Sine 2 G @ 5 ~ 500 Hz, 1 hr/axis
Shock	10G, IEC-68-2-27, half-sine wave, 11 ms duration
Safety	CCC compliant

1.5 Dimensions

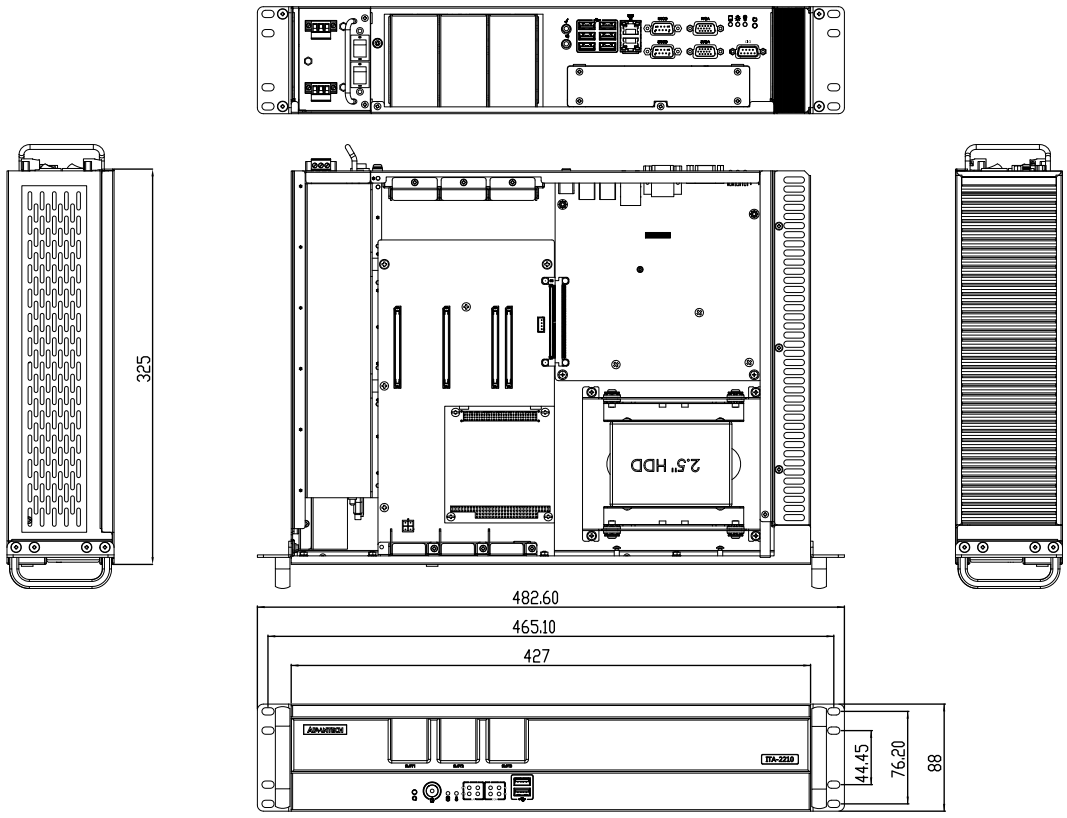


Figure 1.1: ITA-2210 Dimensions Diagram

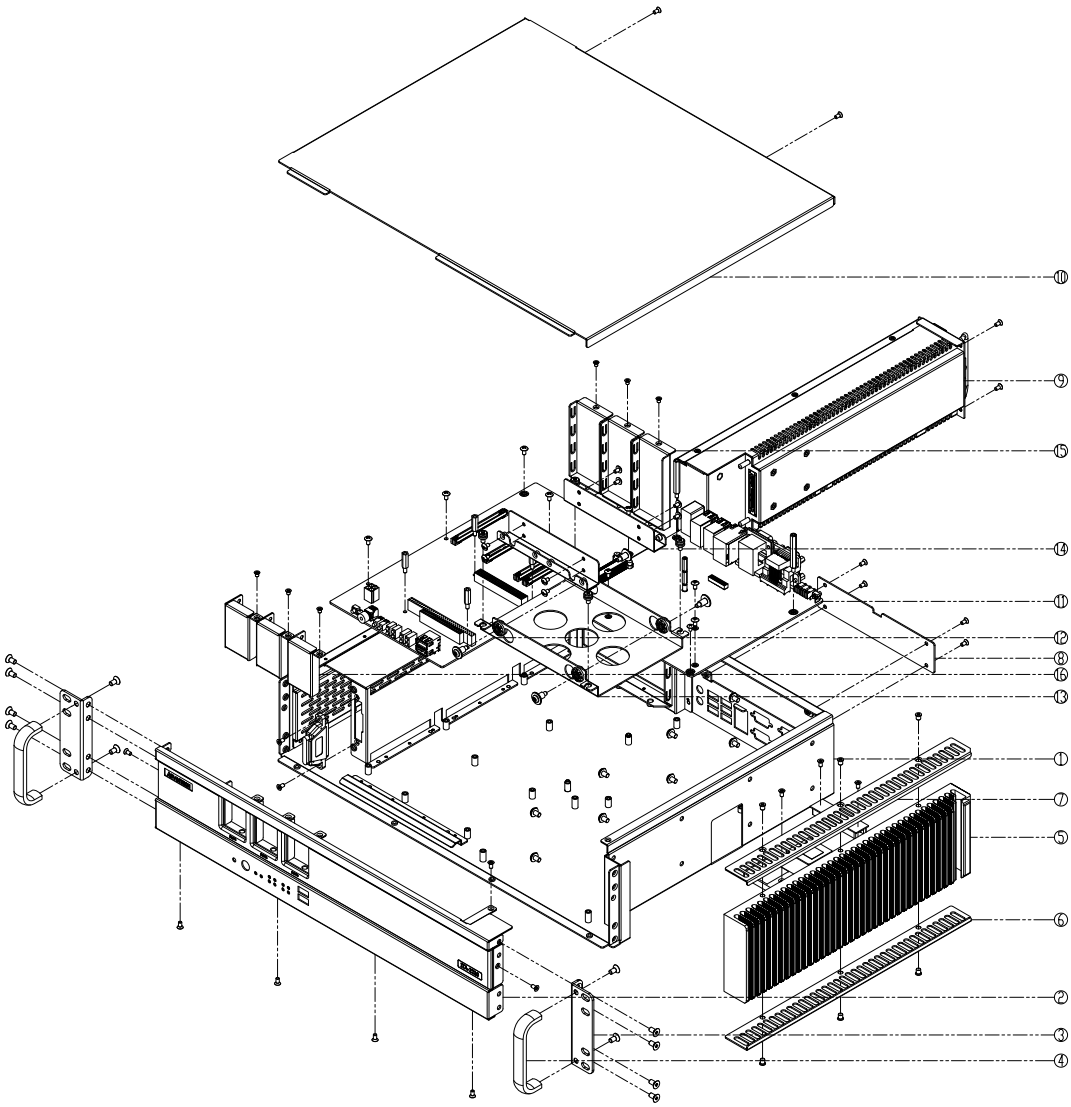


Figure 1.2: ITA-2210 Exploded Diagram

Table 1.3: Parts List			
1	Chassis	9	Power supply module
2	Front panel	10	Top cover
3	Ear	11	Main board
4	Handle	12	Backplane
5	Heat sink	13	3.5" HDD bracket
6	Handguard (down)	14	2.5" HDD bracket
7	Handguard (up)	15	Blank bracket (rear)
8	PC104 blank bracket	16	Blank bracket (front)

Chapter 2

H/W Installation

This chapter provides information regarding the hardware installation.

- Introduction
- System Status Indicators
- Jumpers and Connectors
- I/O Connectors

2.1 Introduction

The following sections detail the internal jumper settings and external connector pin assignments for application integration.

2.2 System Status Indicators

2.2.1 System Status LED Indicators

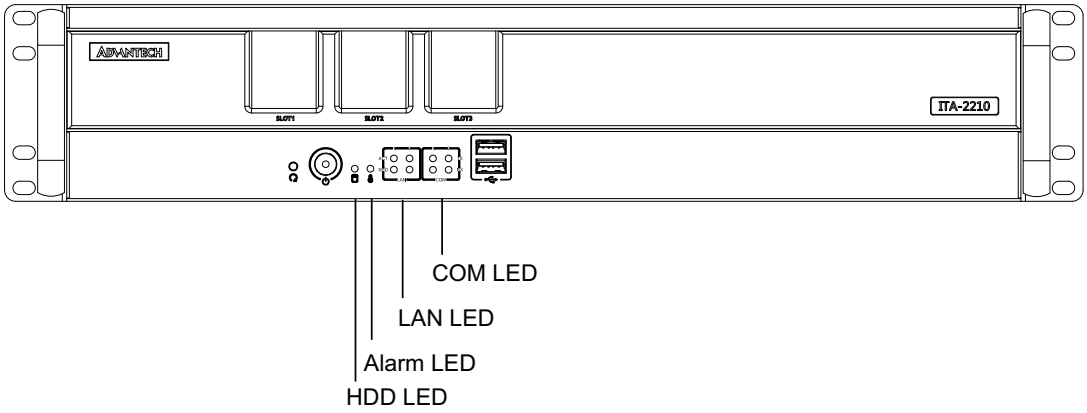


Figure 2.1: Front View of ITA-2210

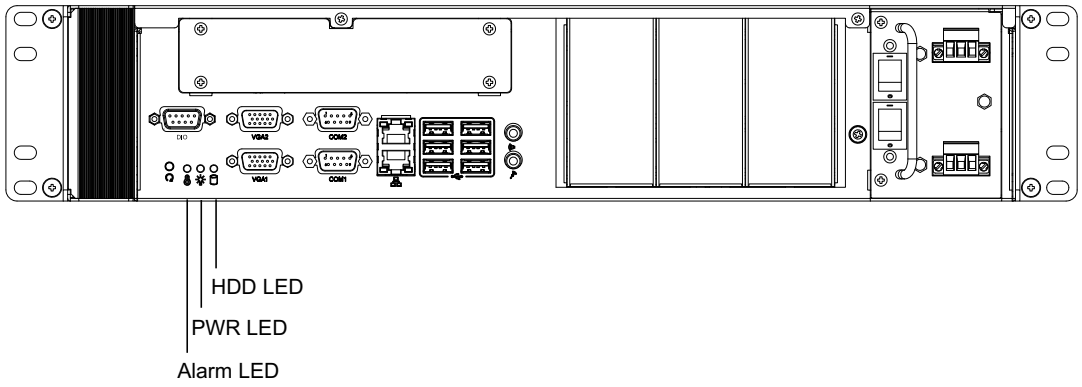


Figure 2.2: Rear View of ITA-2210

2.2.2 System Status LED Indicators

The LEDs located on the lower left of the front and rear panels serve as indicators of system health and transmission status. Please refer to the table below for definitions of the LED behavior.

Item	LED	Status	Color	Description
1	Power	On	Green	System power is on.
		Off		System power is off.
2	Fault	On	Red	System is abnormal.
2	HDD LED	Flickering	Orange	Data is being received / transmitted.
		Off		No data is being received / transmitted.

2.2.3 Ethernet Status LED Indicators

The LEDs located on the lower left of the front panel serve as indicators of Ethernet health and transmission status. Please refer to the table below for definitions of LED the behavior.

Item	LED	Status	Color	Description
1	1000M	On	Green	1000M Data is being received / transmitted.
	100M	On	Orange	100M Data is being received / transmitted.
	10M	Off		10M Data is being received / transmitted.
	Connected	Flickering	Green	Network is being connected.

2.2.4 Serial Port Status LED Indicators

The LEDs located on the lower left of the front panel serve as indicators of the serial port health and transmission status. Please refer to the table below for definitions of the LED behavior.

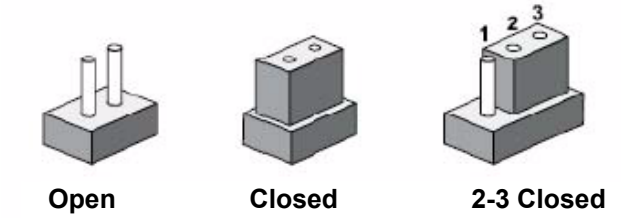
Item	LED	Status	Color	Description
1	TX Active	Flickering	Green	Serial port data is being transmitted.
	TX No Data	Off		No data is being transmitted.
	RX Active	Flickering	Orange	Serial port data is being received.
	RX No Data	Off		No data is being received.

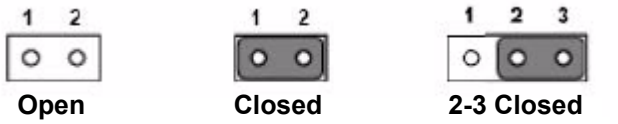
2.3 Jumpers and Connectors

2.3.1 Jumper Description

Users can configure ITA-2210 according to their application needs by setting jumpers. A jumper is a metal bridge used to close an electric circuit. Standard jumpers feature two metal pins and a small metal clip (typically protected by a plastic cover) that slides over the pins to connect them. To close a jumper, simply remove the clip. Certain jumpers feature three pins labelled 1, 2, and 3. With these jumpers, users should connect either Pins 1 and 2, or 2 and 3.

The jumper settings are schematically depicted in this manual as follows:





A pair of needle-nose pliers may be required to adjust jumpers. For advice regarding the optimum hardware configuration for your application, contact your local distributor or sales representative before making any changes. Generally, only a standard cable is required for most connections.

2.3.2 Jumper and Connector Locations

The main board has several connectors and jumpers that facilitate system configuration according to application. The functions of each connector and jumper are listed in Table 2.1. Figs. 2.3 and 2.4 show the jumper and connector locations on the board.

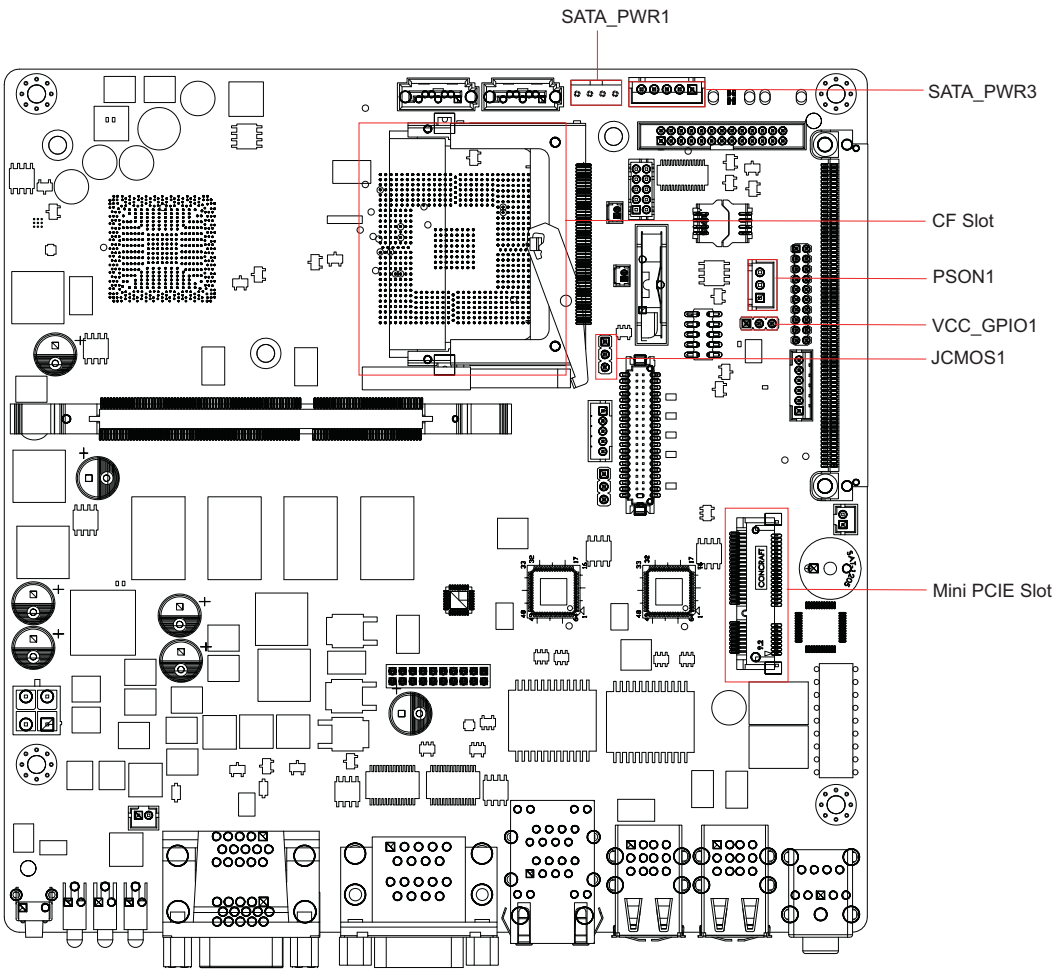


Figure 2.3: Main Board Jumper and Connector Locations

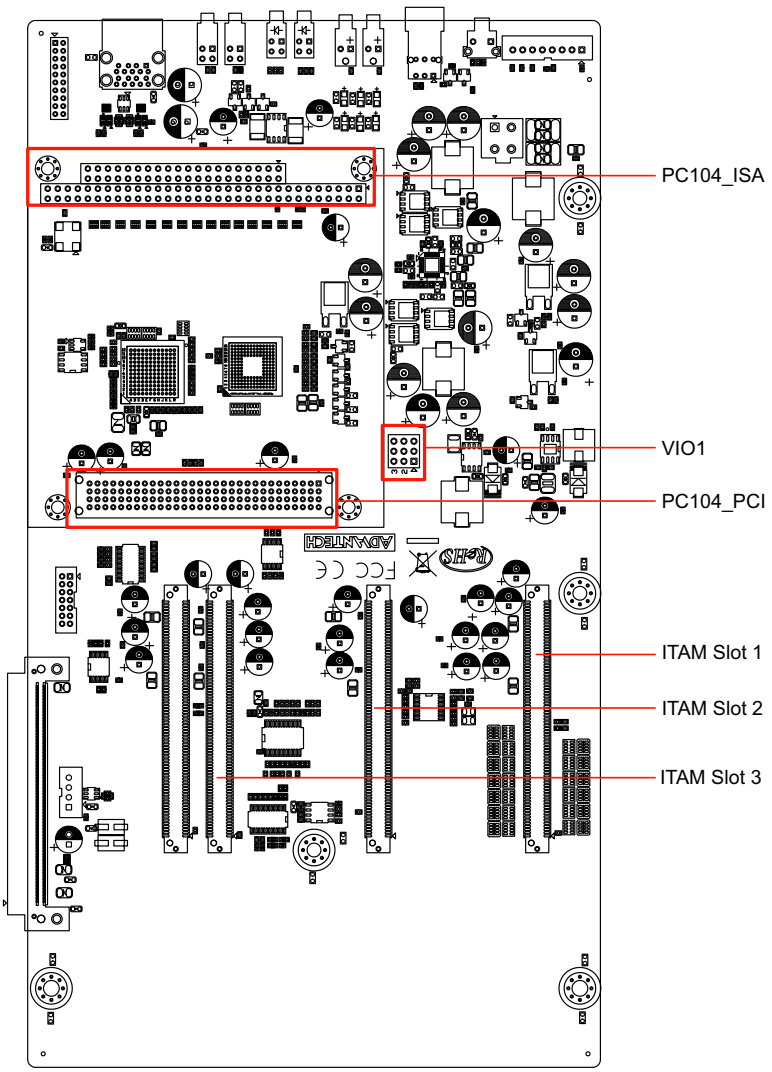
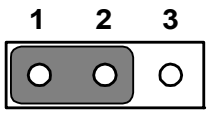


Figure 2.4: Backplane Jumper and Connector Locations

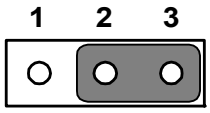
Table 2.1: Jumpers and Internal Connectors

Label	Function
JCMOS1	Clear CMOS settings
VCC_GPIO1	GPIO voltage selection
PSON1	Startup mode selection
VIO1	PCI VIO voltage selection
SATA1	SATA data interface
SATA2	SATA data interface
SATA_PWR1	SATA data interface
SATA_PWR3	SATA data interface

Table 2.2: JCMOS1: Clear CMOS Settings	
Closed Pins	**Results**
1-2	Normal (+V3.3_SB)*
2-3	Clear CMOS settings
* Default	

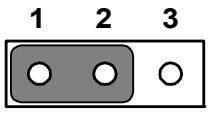


Default

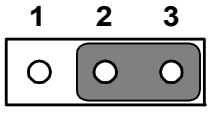


Clear CMOS Settings

Table 2.3: VCC_GPIO1: GPIO Voltage Selection	
Closed Pins	**Results**
1-2	Normal (+V5_SB)*
2-3	+V3.3_SB
* Default	

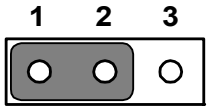


+V5_SB

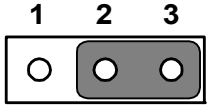


+V3.3_SB

Table 2.4: PSON1: Startup Mode Selection	
Closed Pins	**Results**
1-2	AT mode
2-3*	ATX mode
* Default	



AT Mode



ATX Mode

Table 2.5: VIO1: PCI Voltage Selection	
Closed Pins	**Results**
1-6	Normal (+3.3V)*
4-9	+5V
* Default	

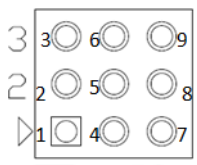


Table 2.6: SATA_PWR1 Pin Settings	
Pin	**Signal Name**
1	+V5
2	GND
3	GND
4	+V12
4P* SATA power cord (Advantech PN: 1700017929).	

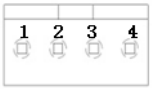
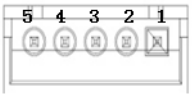


Table 2.7: SATA_PWR3 Pin Settings	
Pin	**Signal Name**
1	+V12
2	GND
3	+V5
4	GND
5	+3.3V
5P* SATA power cord (Advantech PN: 1700022322-01).	



2.4 I/O Connectors

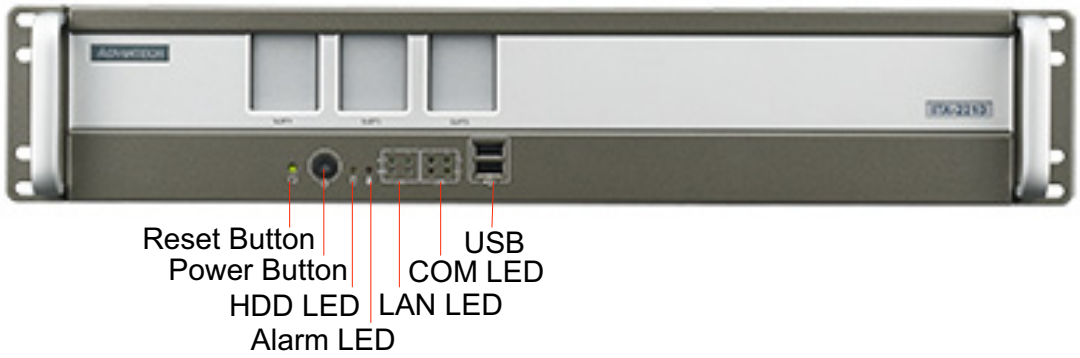


Figure 2.5: Front I/O of ITA-2210

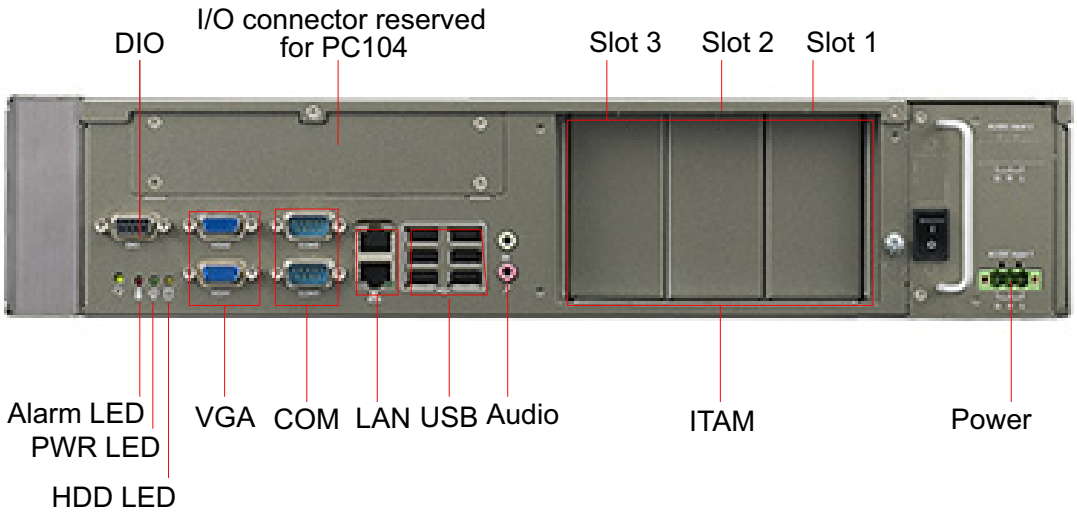
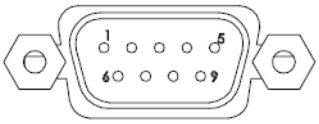


Figure 2.6: Rear I/O of ITA-2210

2.4.1 COM Connector

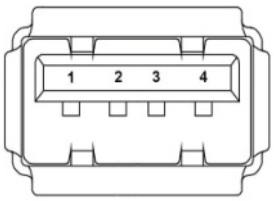
ITA-2210 features two DB 9-pin connectors for RS-232/422/485.



	RS-232	RS-422	RS-485
Pin	**Signal Name**	**Signal Name**	**Signal Name**
1	DCD	Tx-	DATA-
2	RxD	Tx+	DATA+
3	TxD	Rx+	NC
4	DTR	Rx-	NC
5	GND	GND	GND
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.4.2 USB Connector

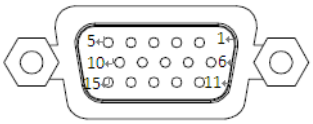
ITA-2210 features eight USB connectors that are USB UHCI, Rev. 2.0 compliant. The USB interface can be disabled in the system BIOS setup utility.



Pin	Signal Name
1	+V5(VCC)
2	USB_data-
3	USB_data+
4	GND

2.4.3 VGA Connector

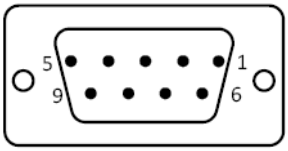
ITA-2210 features two D-sub 15-pin female connectors.



Pin	Signal Name
1	Red
2	Green
3	Blue
4	NC
5	GND
6	GND
7	GND
8	GND
9	+5 V
10	GND
11	NC
12	DDC-DATA
13	H-SYNC
14	V-SYNC
15	DDC-CLK

2.4.4 DIO Connector

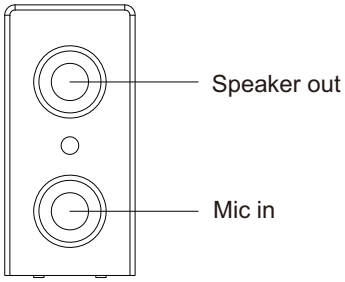
ITA-2210 features one 8-bit DIO, D-sub 9-pin male connector that should be connected via a cable.



Pin	Signal Name	Pin	Signal Name
1	GPIO0	6	GPIO4
2	GPIO1	7	GPIO5
3	GPIO2	8	GPIO6
4	GPIO3	9	GPIO7
5	GND		

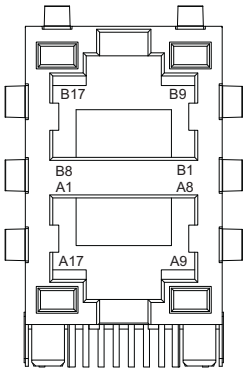
2.4.5 Audio-in Connector

ITA-2210 also features one integrated mic-in / speaker-out audio connector.



2.4.6 LAN Connector

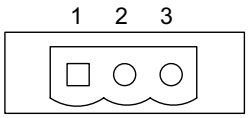
ITA-2210 features two RJ-45 Ethernet connectors (with LEDs indicating network status) that are fully compliant with the IEEE 802.3u 10/100/1000 Mbps standard.



Pin	Signal Name
A1/B1	MDIO0+
A2/B2	MDIO0-
A3/B3	MDIO1+
A4/B4	MDIO2+
A5/B5	MDIO2-
A6/B6	MDIO1-
A7/B7	MDIO3+
A8/B8	MDIO3-

2.4.7 Phoenix Terminal Connector

ITA-2210 features one 3-pin phoenix terminal connector for power input.



Pin	Signal Name
1	GND
2	N
3	L

Chapter 3

System Setup

3.1 Introduction

The procedures for installing modules onto the ITA-2210 system are explained below.

3.1.1 Mainboard CF Card Installation

The ITA-2210 mainboard has a CF card slot on the front panel. Thus, users can insert a CF card into the mainboard directly.

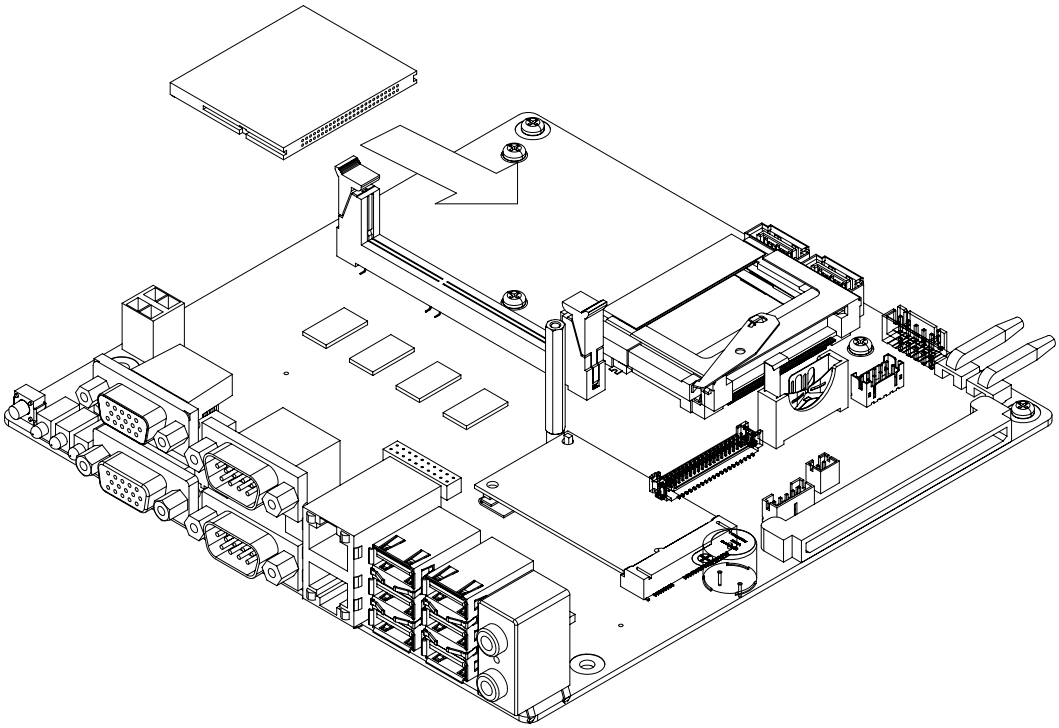


Figure 3.1: Mainboard CF Card Installation

3.1.2 Mini PCIe Card Installation

The ITA-2210 mainboard supports one Mini PCIe expansion card. Please follow the procedures listed below to install the card.

1. Insert a Mini PCIe card into the mainboard PCIE slot.
2. Lock the Mini PCIe card in place using a copper pillar.

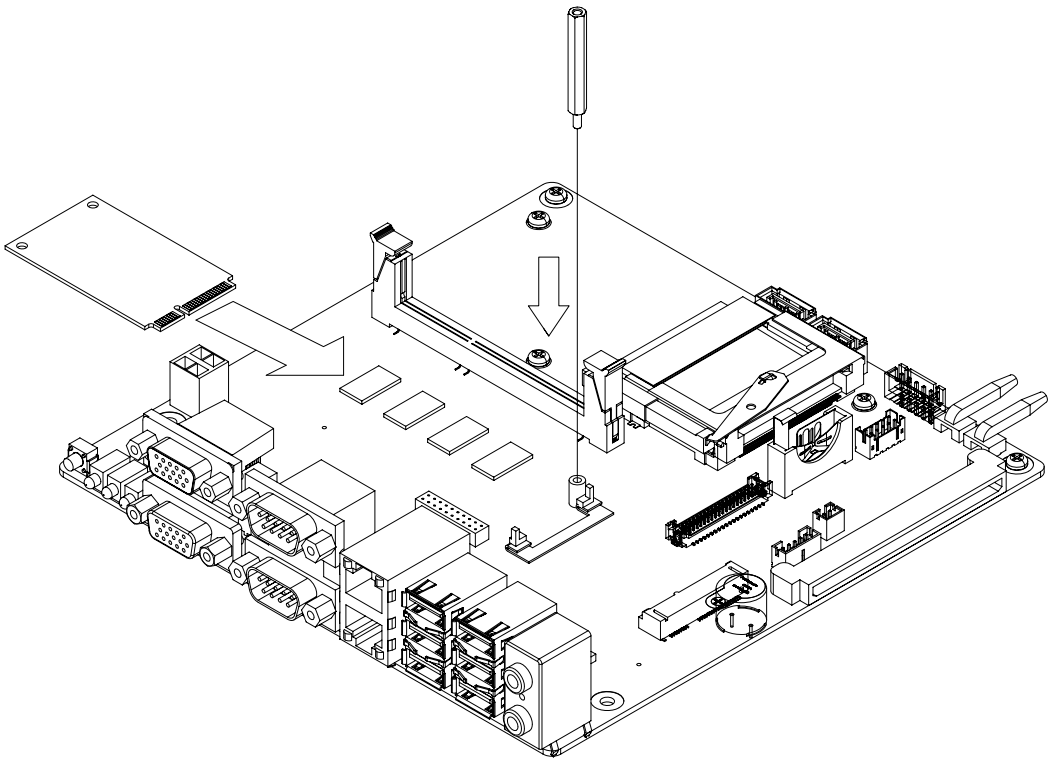


Figure 3.2: Mini PCIe Card Installation

3.1.3 HDD Module Installation

The ITA-2210 is designed with space for a 2.5" or 3.5" HDD module. Please refer to the following instructions to install a hard disk drive.

3.1.3.1 3.5" HDD

1. Remove the top cover (in front of the mainboard) of the chassis and extract the HDD holder.
2. Put the rubber cushions included in the product accessory box into the four holes of the HDD holder.
3. Place a 2.5" HDD (metal side facing upwards) into the HDD holder, ensure that the screw holes on both sides of the HDD are aligned with the center holes of the rubber cushions, then affix the HDD holder using a large screw.
4. Connect a cable to the HDD. Insert the HDD module into the chassis, with the HDD connector facing the backplane, and affix it to the device. Finally, connect the cable from the HDD to the mainboard.

3.1.3.2 2.5" HDD

1. Place a 2.5" HDD into the HDD holder (included in the product accessory box) with the metal side facing upwards. A maximum of two 2.5" HDDs can be installed.
2. Remove the top cover (in front of the mainboard) of the chassis and extract the HDD holder.
3. Put the rubber cushions included in the accessory box into the four holes of HDD holder.
4. Place the assembled 2.5" HDD module into the HDD holder and affix it using a large screw.
5. Connect a cable to the HDD. Insert the HDD module into the chassis, with the HDD connector facing the backplane, and affix it to the device. Finally, connect the cable from the HDD to the mainboard.

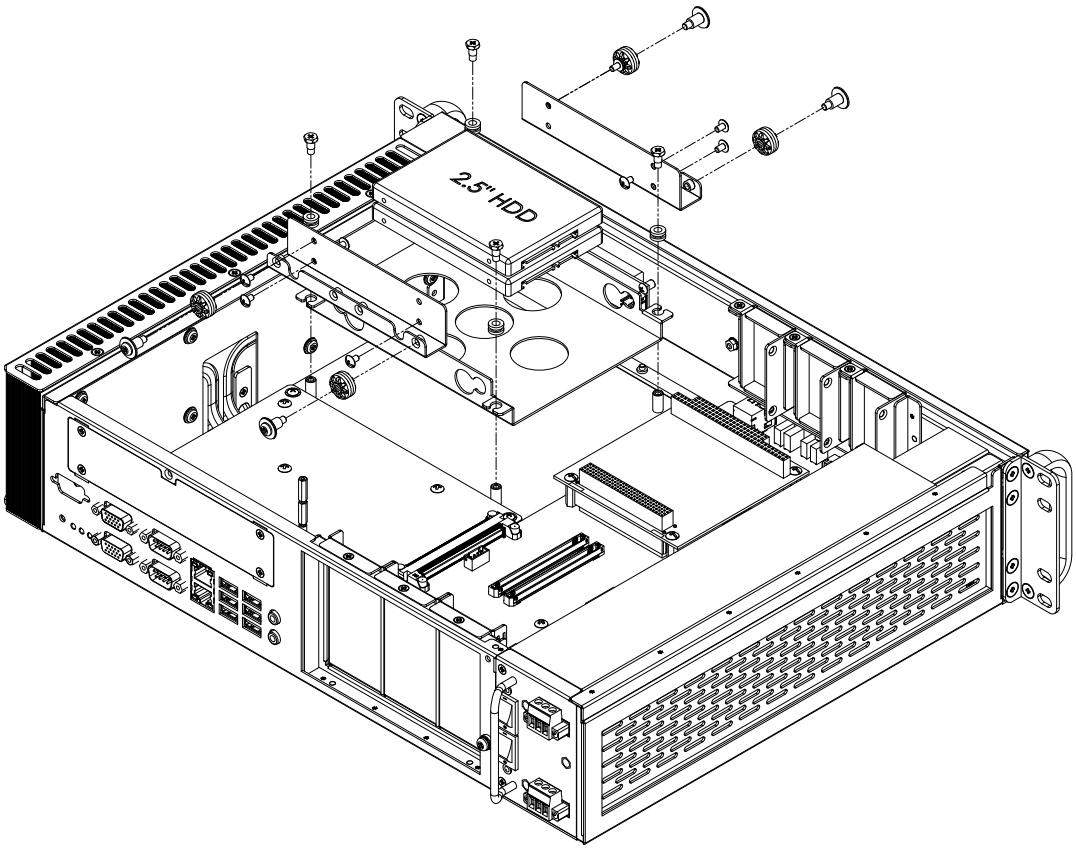


Figure 3.3: HDD Module Installation

3.1.4 Top Cover Installation

Follow the procedures outlined below to install the chassis top cover.

1. Insert the notch end of the top cover into the front panel of the chassis, as shown in Fig. 3.4, and press firmly.
2. Affix the chassis top cover using two screws.

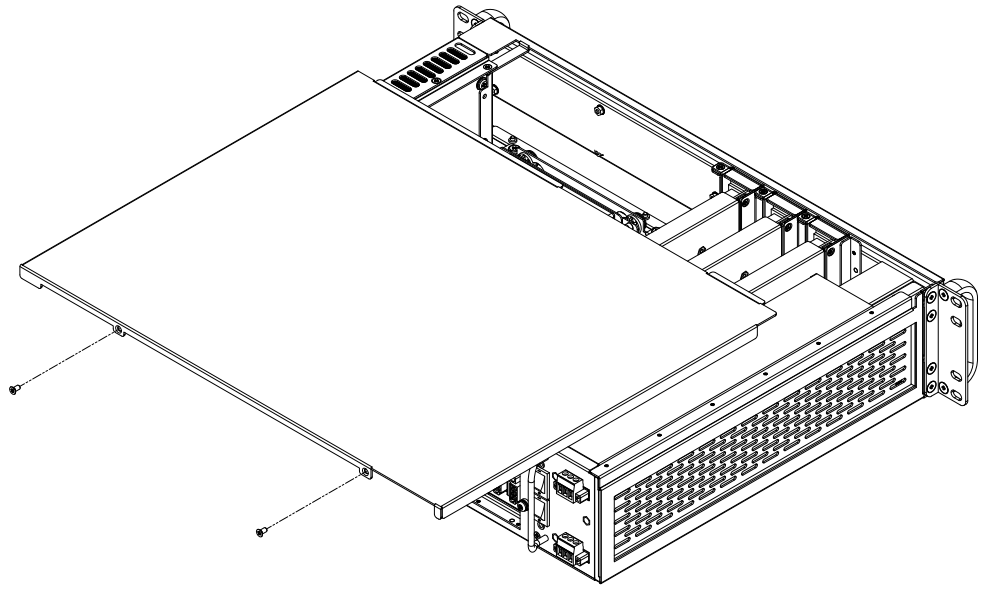


Figure 3.4: Top Cover Installation

3.1.5 Ear and Handle Installation

Align the screw holes of the ears with the holes on the chassis, then use screws to affix the ears in place. Next, align the screw holes of the handles with those of the ears, and use screws to affix the handles in place (see Fig. 3.5).

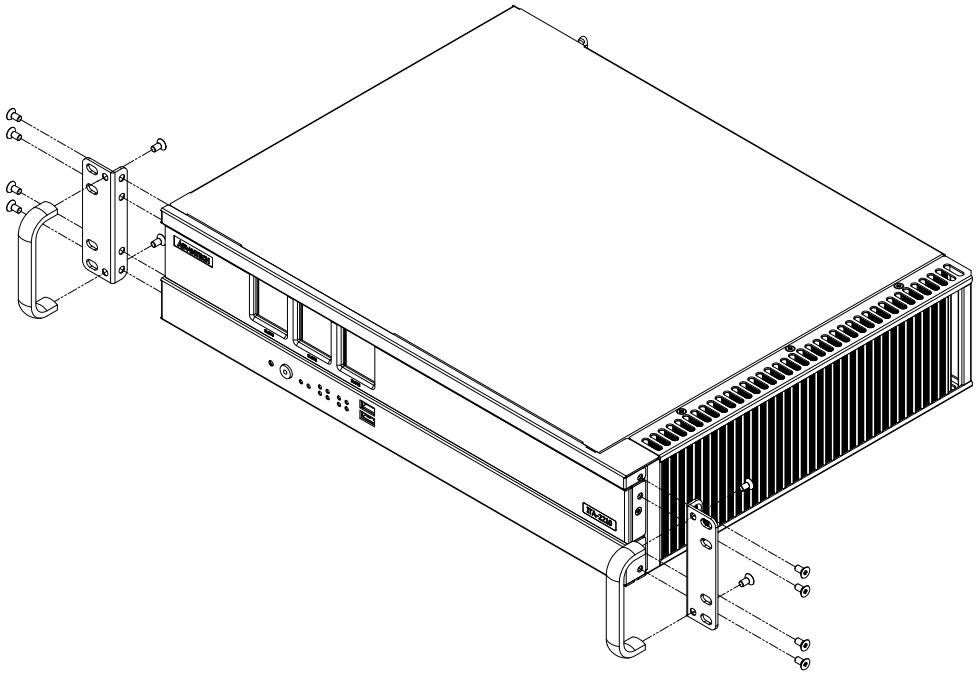


Figure 3.5: Ear and Handle Installation

3.1.6 ITAM Card Module Installation

Follow the procedures listed below to install the ITAM card module.

1. Remove the top cover of the ITA-2210 chassis.
2. Insert the ITAM module as shown in Fig. 3.6.

a. Insert the module I/O into the I/O panel of the chassis.
b. Affix the front side of the module to the front panel of the chassis.
c. Check whether the ITAM module connector is parallel to the ITAM slot on the backplane.
d. Ensure that the module is fully inserted.

3. Affix the ITAM module in the ITA-2210 system using screws.

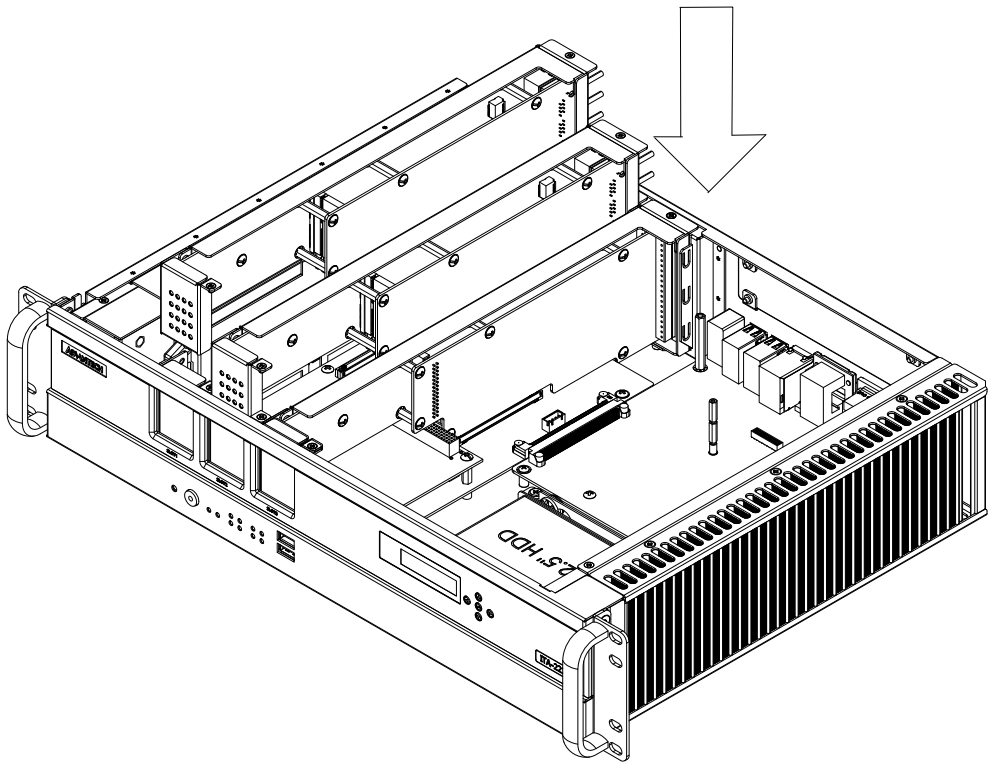


Figure 3.6: ITAM Card Module Installation

Note:

ITA-2210 and ITA-2230 can support a maximum of 14 devices in Windows XP (the number and type of devices are not limited in Linux).

The combination of Windows XP supports is shown in the following table:

ITAM Module	Occupied Device Count	Max Combination When All Card Slots Are Occupied
ITAM-SR01	1	ITAM-SR01 x 3 ITAM-NC01 x1 + ITAM-SR01 x 2 ITAM-NC02 x 1 + ITAM-SR01 x 2 ITAM-NC02 x 2 + ITAM-SR01 x 1
ITAM-NC01-C	9	
ITAM-NC02-C	5	
ITAM-NC02-F	5	
On-board LAN	2	

Chapter 4

AMI BIOS Setting

This chapter explains the AMI BIOS configuration process.

4.1 Introduction

AMIBIOS has been integrated into numerous motherboards for over a decade. This chapter explains how to configure the AIM BIOS for the ITA-2210 series. Using the AMIBIOS Setup program, users can modify the BIOS settings and control special computer features. The Setup program comprises several menus with options for adjusting the computer settings and enabling or disabling special features. The basic navigation of the ITA-2210 BIOS Setup Utility is described in this chapter.

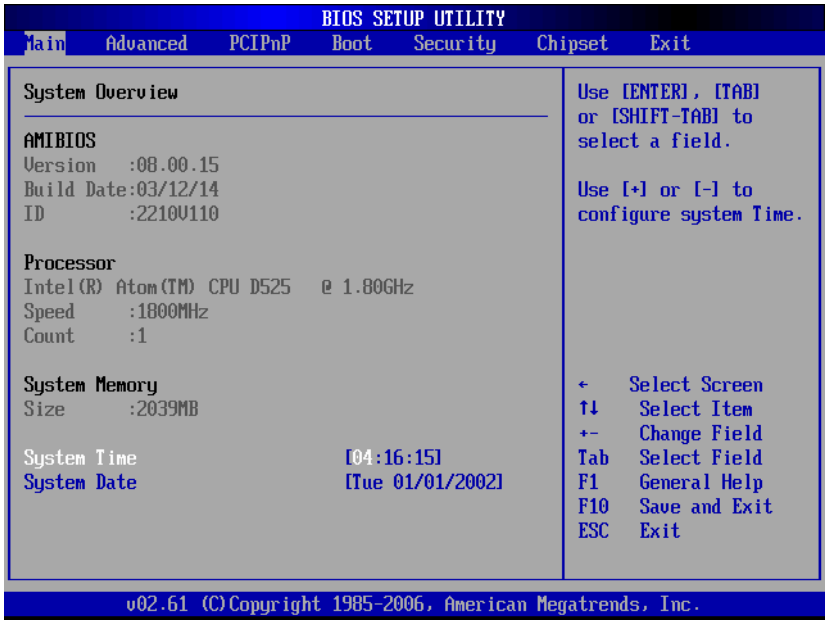


Figure 4.1: BIOS Setup Utility Landing Page

AMI's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed up CMOS so it retains the Setup information when the power is turned off.

4.2 Entering Setup

Turn on the computer to enter the power-on self-test (POST) screen where the BIOS and CPU information is displayed. Press <Del> to enter Setup.

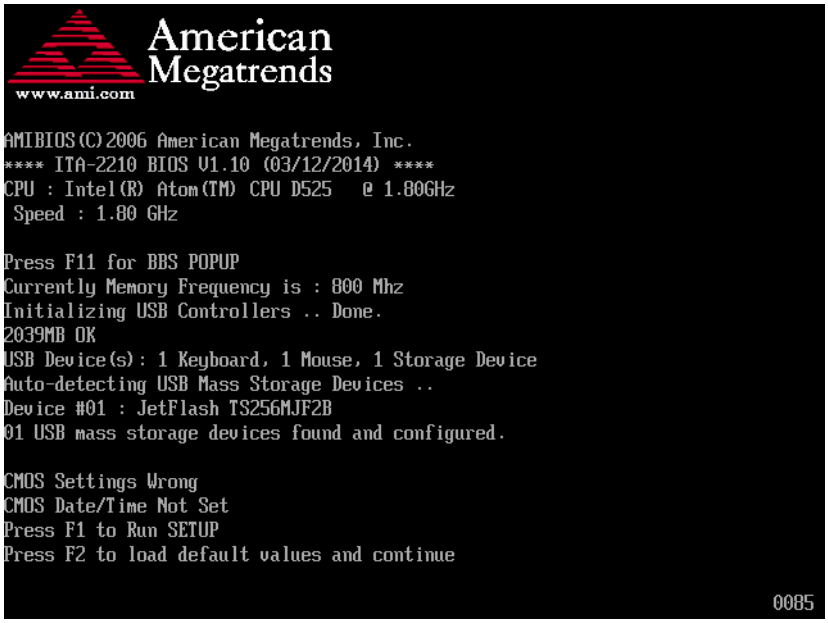


Figure 4.2: Press <Del> to Enter Setup

4.2.1 Main Setup

When first entering the BIOS Setup Utility, users will land on the Main setup page. Users can always return to the Main setup page by selecting the Main tab. The Main setup page features two setup options, which are explained in this section. The Main BIOS setup page is shown below.

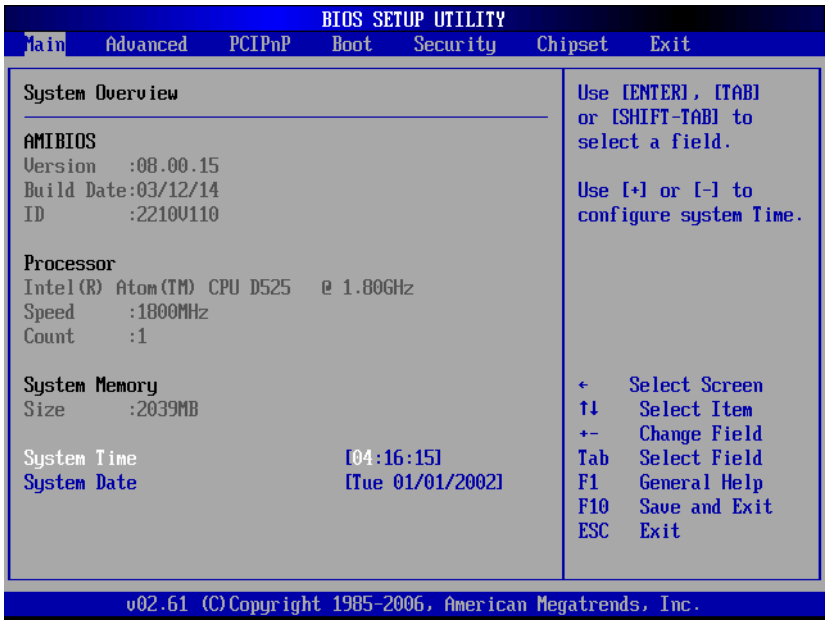


Figure 4.3: Main BIOS Setup Page

The Main BIOS setup page comprises two main frames. The left frame displays all configurable options. The grayed-out options cannot be configured, whereas the options in blue can be. The right frame shows the key legend.

The area above the key legend is reserved for text messages. When an option is selected in the left frame, the text display color changes to white and is typically accompanied by a text message.

- **System Time / System Date**
  Use this option to change the system time and date. Highlight the System Time or System Date options using the <Arrow> keys. Input new values using the keyboard. Press the <Tab> or <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format, and the time must be entered in HH:MM:SS format.

4.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the ITA-2210 BIOS setup screen to access the Advanced BIOS setup page. Select any item in the left frame of the page, f9or example, CPU Configuration, to open the submenu for that item. Users can select an Advanced BIOS setup option by highlighting it using the <Arrow> keys. All Advanced BIOS setup options are described in this section. The images below show the Advanced BIOS setup page. The submenus for each item are described in the following pages.

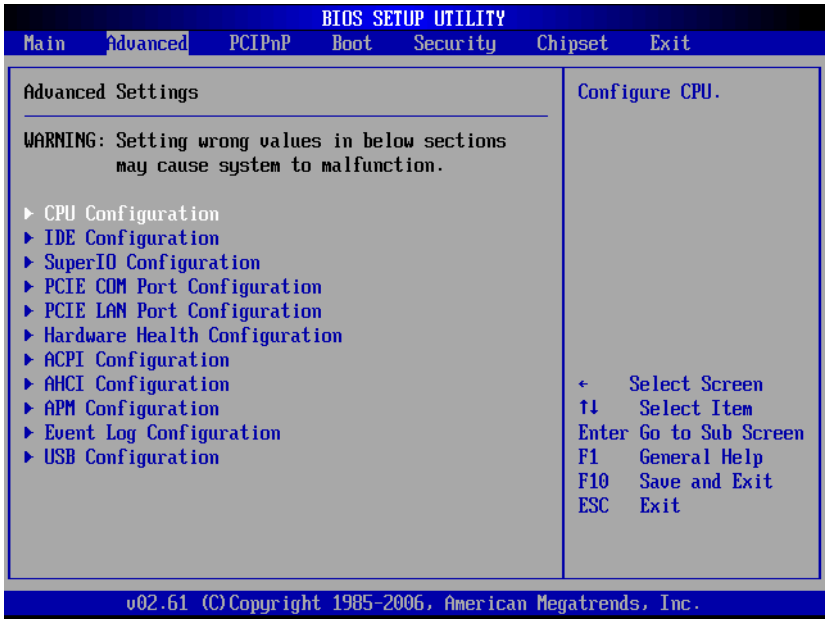


Figure 4.4: Advanced BIOS Features Setup Page

4.2.2.1 CPU Configuration

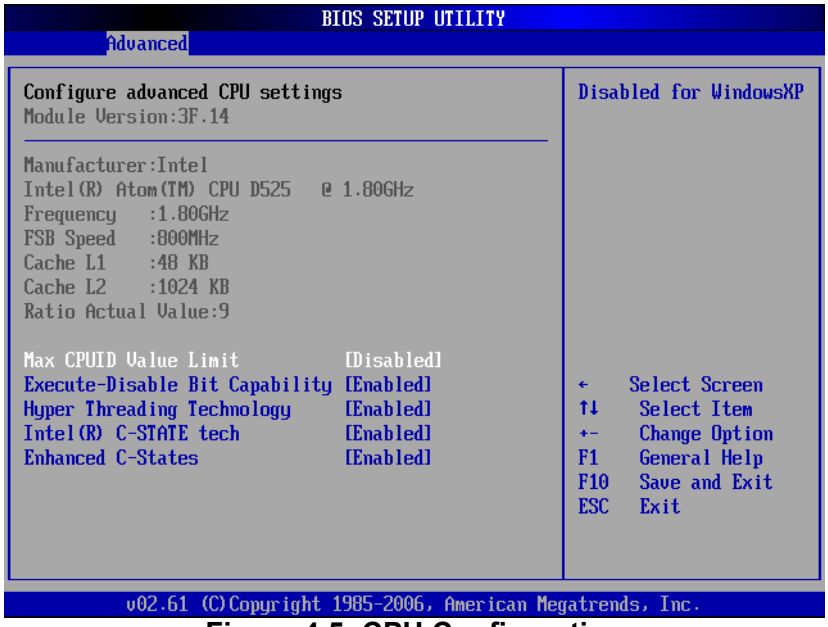


Figure 4.5: CPU Configuration

- **Max CPUID Value Limit**
  This item allows users to configure the maximum CPUID value.
- **Execute-Disable Bit Capability**
  This item allows users to enable or disable the Execute Disable Bit feature. The default setting is “Enabled”.
- **Hyper Threading Technology**
  This item allows users to enable or disable Intel® Hyper Threading Technology. The default setting is “Enabled”.
- **Intel® C-STATE Technology**
  This function reduces the power consumed by the CPU in system halt states.
- **Enhanced C-States**
  This item allows users to enable or disable C-states. The default setting is “Enabled”.

4.2.2.2 IDE Configuration

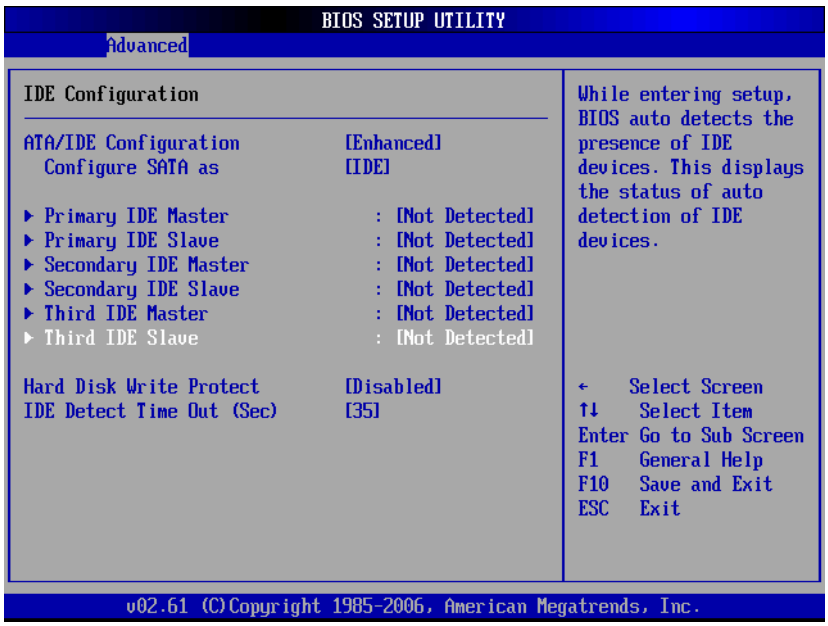


Figure 4.6: IDE Configuration

- **IDE Configuration**
  The default setting is “Enabled”, which means all SATA resources are enabled.
- **Enhanced Mode**
  Two options exist for this mode: IDE and AHCI. The default setting is “IDE”.
- **Primary / Secondary / Third / Fourth IDE Master and Slave**
  When initialized, the BIOS Setup Utility auto detects the presence of IDE devices and displays their status.
  - Type: Select the SATA driver type. The options are “Not Installed”, “Auto”, “CD / DVD”, and “ARMD”.
  - LBA / Large Mode: Enable or disable LBA mode.
  - Block (Multi-Sector Transfers): Enable or disable multi-sector data transfers.
  - PIO Mode: Select PIO mode.
  - DMA Mode: Select DMA mode.
  - S.M.A.R.T.: Select Self-Monitoring, Analysis, and Reporting Technology
  - 32-Bit Data Transfers: Enable or disable 32-bit data transfers.
- **Hard Disk Write Protection**
  This item allows users to enable or disable the device write protection feature. This item is only available when accessing the device via the BIOS, and is only effective in DOS. The default configuration is “Disabled”.
- **IDE Detect Time Out (Sec)**
  This item allows users to detect the ATA / ATAPI device time out value. The default value is “35”.

4.2.2.3 Super I/O Configuration

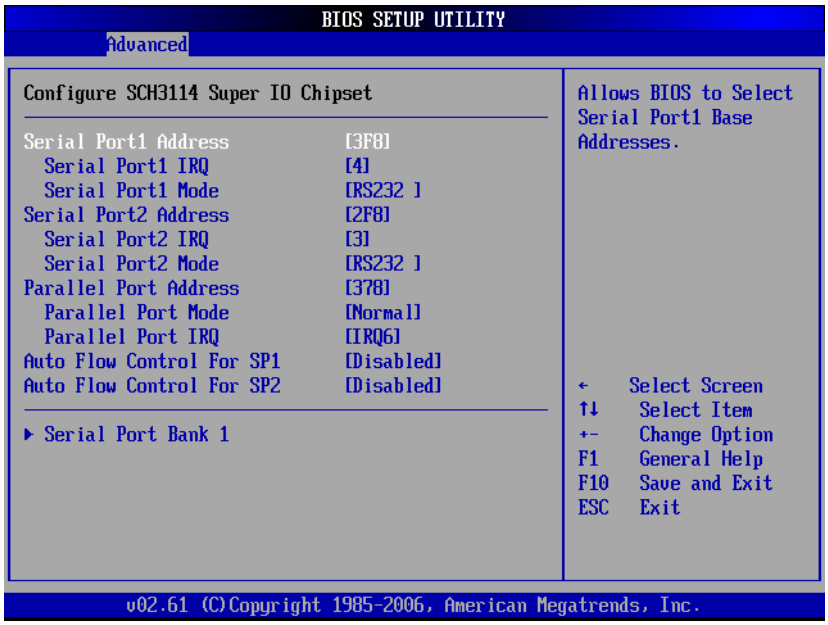


Figure 4.7: Super I/O Configuration

- **Serial Ports 1 and 2 Address, IRQ, and Mode settings**

  These items allow users to configure the base address and IRQ for Serial Ports 1 and 2, as well as enable RS-232/422/485 modes.

- **Parallel Port Address, IRQ, and Mode settings**

  These items allow users to configure the parallel port base address and IRQ, as well as enable RS-232/422/485 modes.

- **Auto Flow Control For Serial Port 1**

  This item allows users to configure the 485 protocol for Serial Port 1. Options are “Enabled” and “Disabled”.

- **Auto Flow Control For Serial Port 2**

  This item allows users to configure the 485 protocol for Serial Port 2. Options are “Enabled” and “Disabled”.

4.2.2.4 PCIE COM Port Configuration

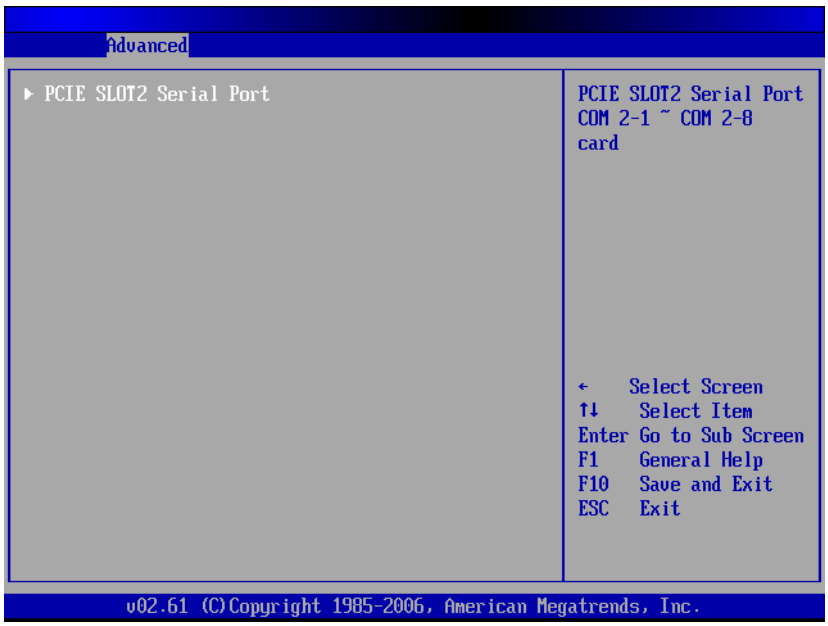


Figure 4.8: PCIE Slot 2 Serial Port

- **PCIE Slot 2 Serial Port**
  This item allows users to access the serial port information for the second PCIE slot. ITA-2210 has three PCIE slots for the ITAM I/O expansion module. However, only the card information for Slot 2 is displayed.

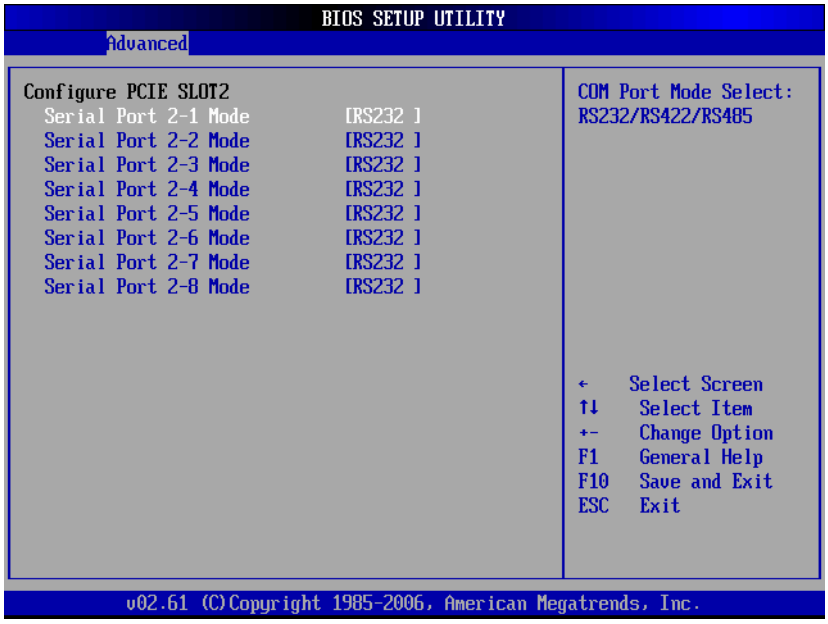


Figure 4.9: PCIE Slot 2 Configuration

- **PCIE Slot 2 Serial Port**
  This item allows users to access the serial port information for the second PCIE slot. Users can select the serial port and Mode 2-1 to Mode 2-8 to enable RS232/RS422/RS485. RS485 supports the Flow Control function, which is managed by the driver and should be configured within the driver.

4.2.2.5 PCIE LAN Port Configuration

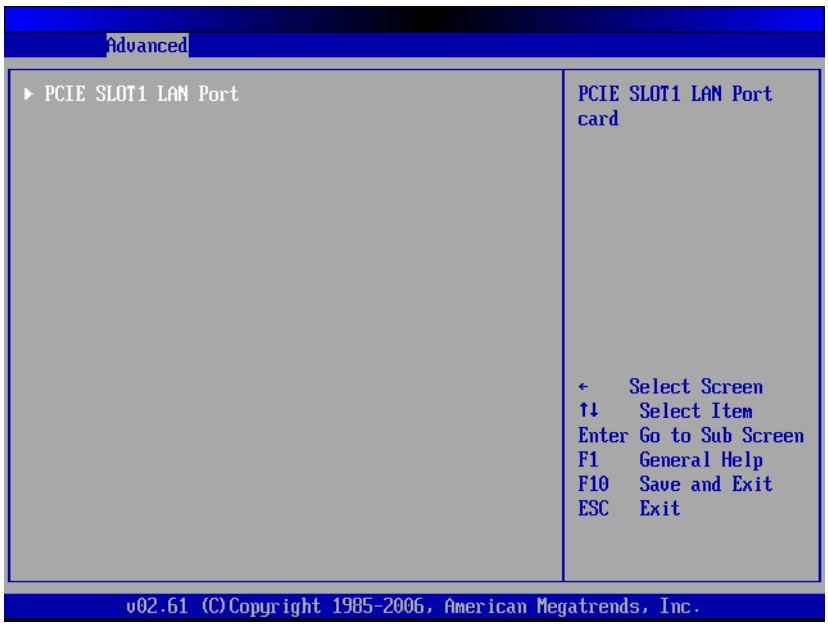


Figure 4.10: PCIE Slot 1 LAN Port

- **PCIE Slot 1 LAN Port**
  This item allows users to access the serial port information for the first PCIE slot. ITA-2210 has three PCIE slots for the ITAM I/O expansion module. However, only the card information for Slot 1 is displayed.

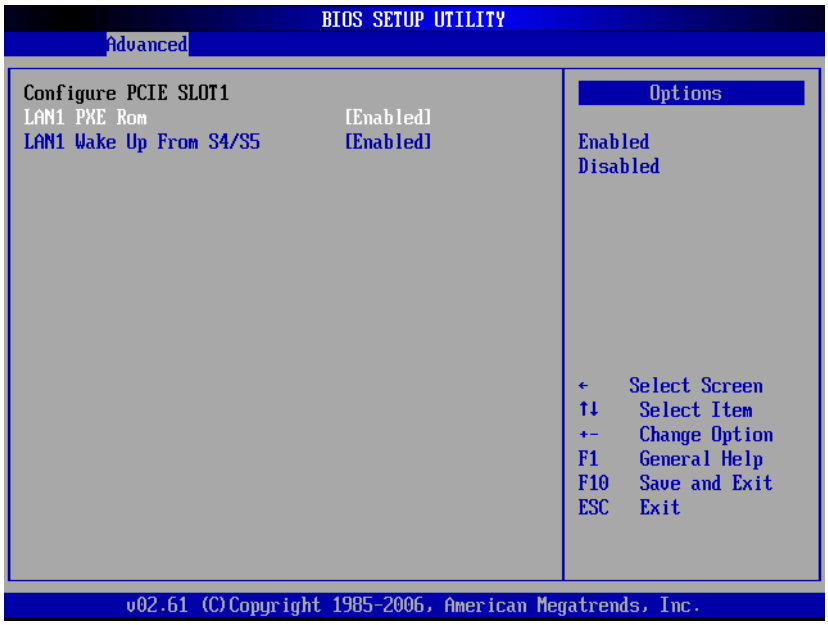


Figure 4.11: PCIE Slot 1 Configuration

- **LAN1 PXE Rom**
  This item allows users to enable or disable the LAN1 PXE Rom.
- **LAN1 Wake Up From S4/S5**
  This item allows users to enable or disable the function of LAN 1 wake up from S4/S5.

4.2.2.6 Hardware Health Configuration

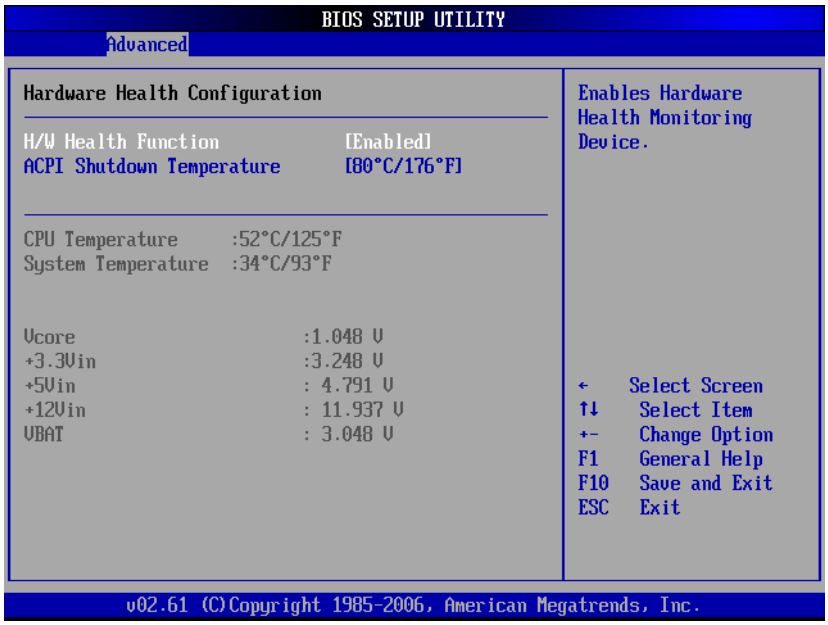


Figure 4.12: Hardware Health Configuration

- **H/W Health Function**

  This item allows users to enable the hardware monitoring function.

- **ACPI Shutdown Temperature**

  This item allows users to set the ACPI shutdown temperature threshold. When the shutdown temperature is reached, the system shuts down automatically to protect the device from damage due to overheating. Users can also view the system temperature, CPU temperature, and fan states on this page.

4.2.2.7 ACPI Configuration

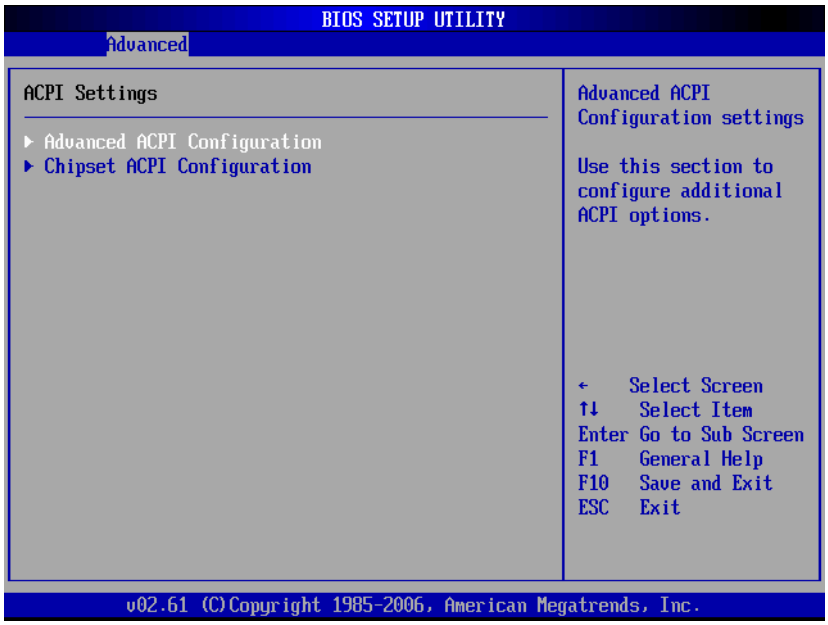


Figure 4.13: ACPI Settings

- **Advanced ACPI Configuration**
  This item allows users to configure additional ACPI options.

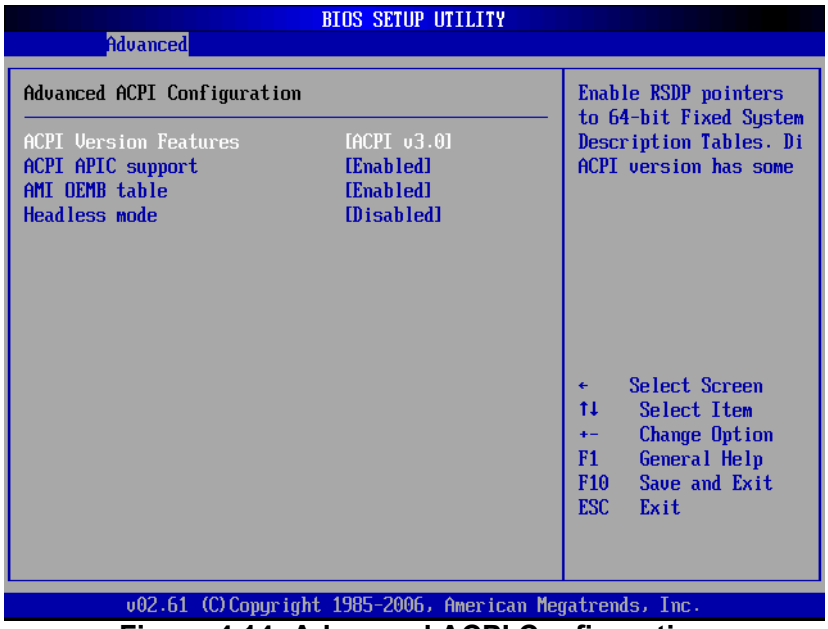


Figure 4.14: Advanced ACPI Configuration

- **ACPI Version Features**
  This item allows users to enable the RSDP pointer for a 64-bit fixed system specification table. Set this item to allow or forbid system compliance with ACPI 1.0/2.0/3.0 specifications.
- **ACPI APIC Support**
  This item allows users to enable or disable a table pointer from aligning the RSDT pointer. The default setting is “Enabled”.
- **AMI OEMB Table**
  This item allows users to enable or disable the ACPI OEMB table pointer from aligning the RSDT pointer. The default setting is “Enabled”.
- **Headless Mode**
  This item allows users to enable or disable Headless mode using ACPI. The default setting is “Disabled”.
- **Chipset ACPI Configuration**
  This item allows users to configure the chipset ACPI.

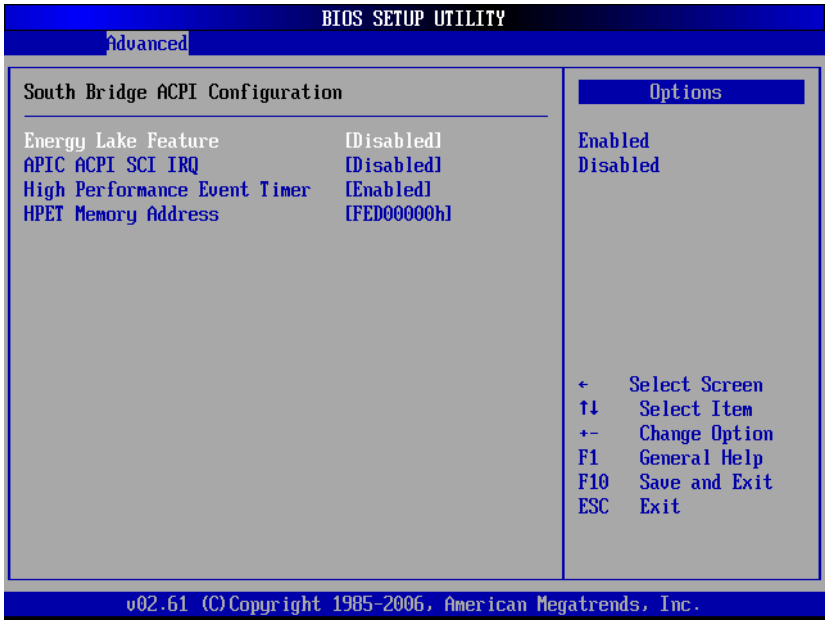


Figure 4.15: Chipset ACPI Configuration

- **Energy Lake Feature**
  Can be enabled or disabled. The default setting is “Disabled”.
- **APIC ACPI SCI IRQ**
  Can be enabled or disabled. The default setting is “Disabled”.
- **High performance Event Timer**
  Can be enabled or disabled. The default setting is “Disabled”.
- **HPET Memory Address**
  This item allows users to set the HPET memory address. The default setting is “FED00000h”.

4.2.2.8 AHCI Configuration

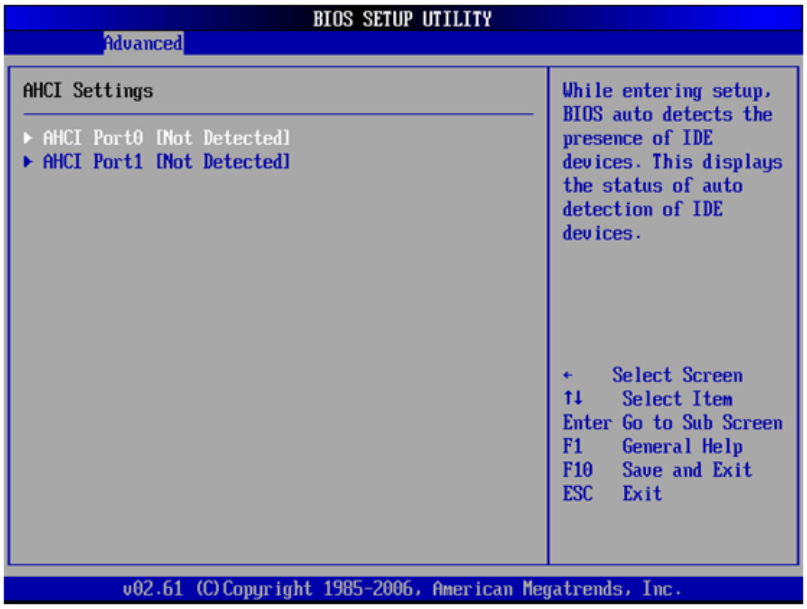


Figure 4.16: AHCI Configuration

- **AHCI Ports 0 and 1 Detection**

  When initialized, the BIOS Setup Utility automatically detects SATA devices and displays the status of existing SATA devices.

  – Type: Select the device to system connection type. The options are “Not Installed” and “Auto”.

  – S.M.A.R.T.: Select Self-Monitoring, Analysis, and Reporting Technology.

4.2.2.9 APM Configuration

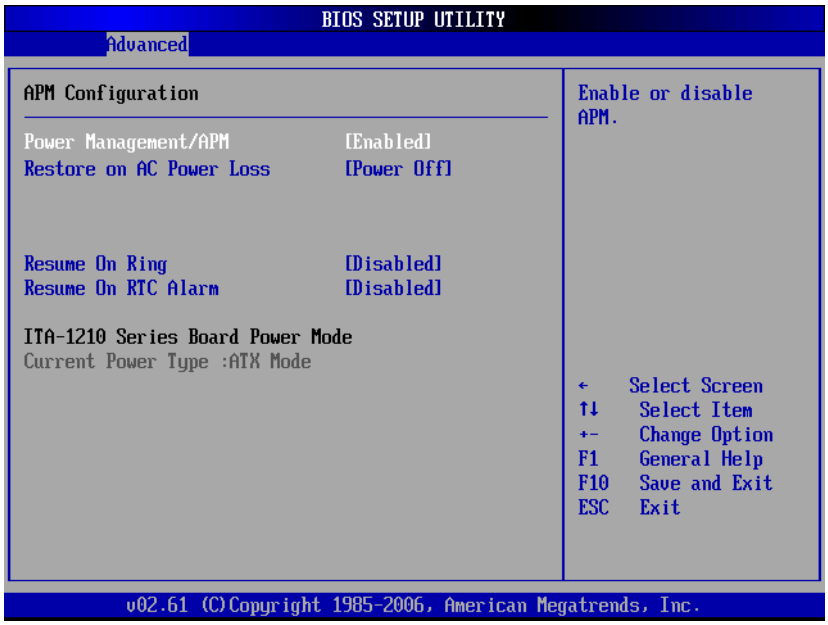


Figure 4.17: APM Configuration

- **APM Configuration**
  This item comprises the following five options:
  - Power Management / APM
    Options are “Disabled” and “Enabled”. The default setting is “Enabled”.
  - Power Button Mode
    Options are “On / Off” and “Suspend”. The default setting is “On / Off”.
  - Restore on AC Power Loss
    Options are “Power Off”, “Power On”, and “Previous State”. The default setting is “Power Off”.
  - Resume on Ring
    Options are “Disabled” and “Enabled”. The default setting is “Disabled”.
  - Resume on RTC Alarm
    Options are “Disabled” and “Enabled”. The default setting is “Disabled”.
- **ITA-2210 Series Power Mode**
  This item allows users to detect whether the current power mode is set to AT or ATX mode.

4.2.2.10 Event Log Configuration

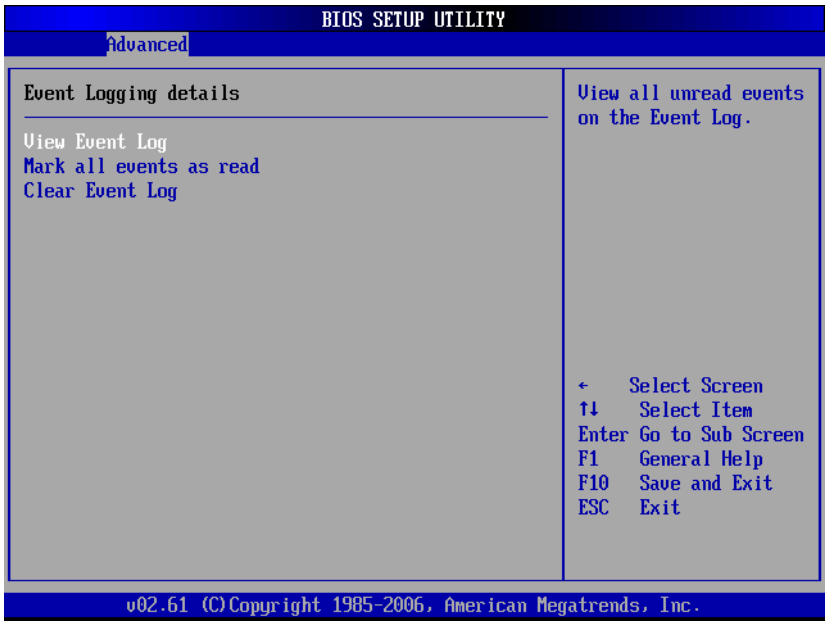


Figure 4.18: Event Log Configuration

- **View Event log**

  This item allows users to view all unread events in the event log, including the errors and warnings displayed during the BIOS startup process.

- **Mark All Events as Read**

  This item allows users to mark all unread events as read. The last option is “No Unread Log”.

- **Clear Event Log**

  This item allows users to clear all unread log events, and consider them as read. The first option is “No Unread Log”.

4.2.2.11 USB Configuration

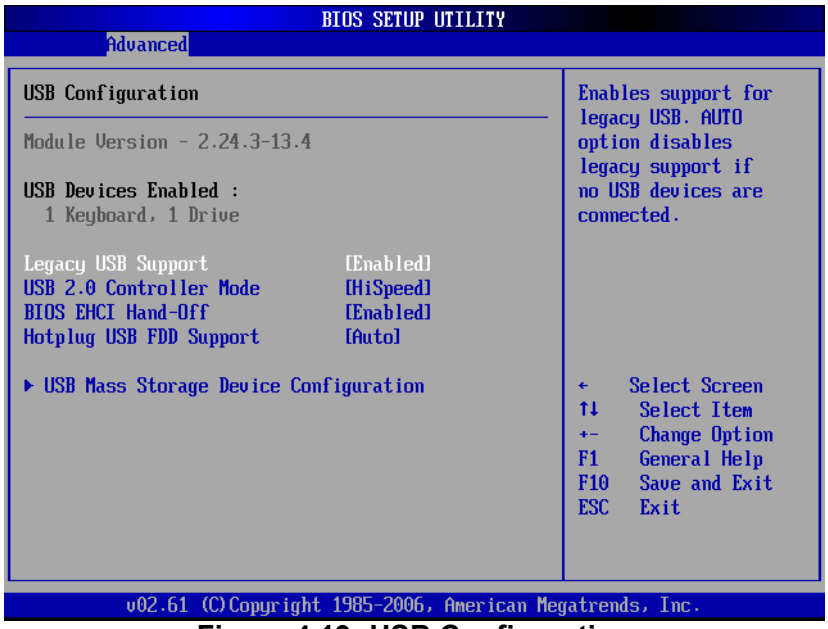


Figure 4.19: USB Configuration

- **Legacy USB Support**

  This item allows users to enable support for standard USB. The default setting is "Enabled". The item setting automatically changes to "Disabled" when no USB device is connected.

- **USB 2.0 Controller Mode**

  Options are "Hi Speed" and "Full Speed". The default setting is "Hi Speed".

- **BIOS EHCI Hands Off**

  This item allows users to enable support for OS without hands-off functionality.

- **Hotplug USB FDD Support**

  The system creates a virtual FDD device connected to a hot-swap FDD. This virtual device is only automatically generated when no USB FDD exists.

- **USB Mass Storage Device Configuration**

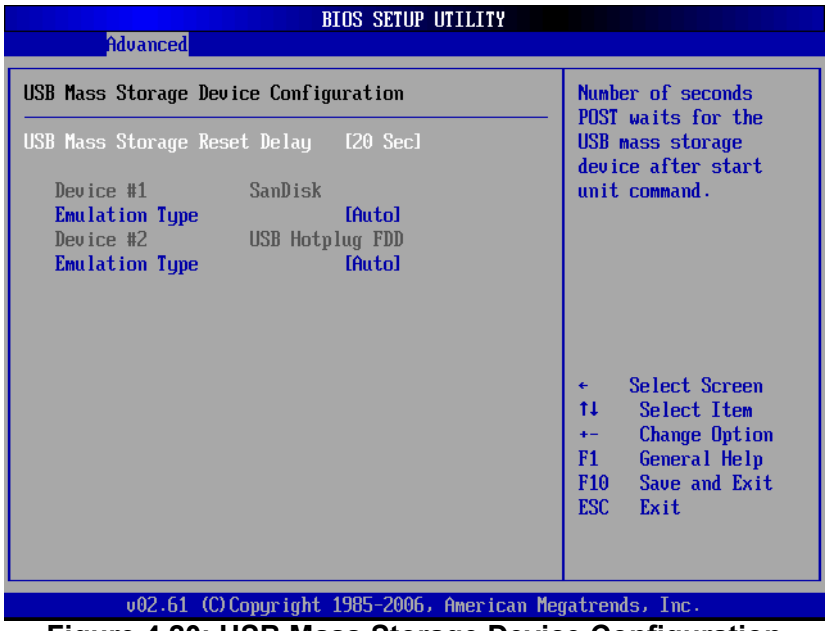


Figure 4.20: USB Mass Storage Device Configuration

– USB Mass Storage Reset Delay

POST time (seconds) of USB mass storage after initiating the unit command.

– USB Device Emulation Type

This item allows users to set the simulation type for a specific USB device. The options are “Auto”, “Floppy”, “Forced FDD”, “Hard Disk”, and “CD-ROM”.

If set to “Auto”, USB devices smaller than 530 MB are simulated as FDD, and others are simulated as HDD. If set as “Forced FDD”, FDD format drives can be activated as FDD, such as ZIP drives.

4.2.3 PCI / PnP Setup

Select the PCI/PnP tab from the ITA-2210 BIOS setup screen to access the PnP BIOS setup page. Users can select a PnP setup option by highlighting it using the <Arrow> keys. All PnP BIOS Setup options are described in this section. The PnP BIOS setup page is shown below.

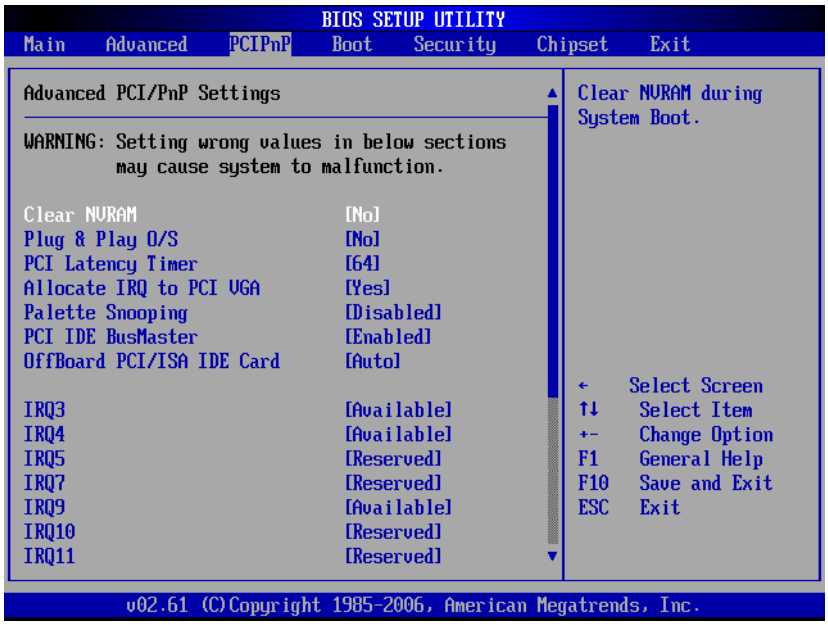


Figure 4.21: PCI / PnP BIOS Setup Page

- **Clear NVRAM**

  Set this value to force the BIOS to clear the non-volatile random access memory (NVRAM). This is set as “No” for both the Optimal and Fail-Safe default settings.

- **Plug and Play O/S**

  When set as “No”, the BIOS configures all devices in the system. When set as “Yes”, if users have installed a PnP O/S, the O/S configures the PnP devices that do not require initiating. The default setting is “No”.

- **PCI Latency Timer**

  This item allows users to adjust the PCI Latency Timer. The configuration of this item determines the latency of all PCI devices on the PCI bus. This item is set as “64” for both the Optimal and Fail-Safe default settings.

- **Allocate IRQ to PCI VGA**

  This item allows users to enable or disable the system from providing the VGA adapter card with an interrupt address. This item is set as “Yes” for both the Optimal and Fail-Safe default settings.

- **Palette Snooping**
- Set this value to allow the system to modify the Palette Snooping settings. This item is set as “Disabled” for both the Optimal and Fail-Safe default settings.
- **PCI IDE Busmaster**

  This item allows users to enable or disable the use of PCI IDE busmastering. This is set as “Disabled” for both the Optimal and Fail-Safe default settings.
- **OffBoard PCI/ISA IDE Card**

  Set this value to allow an add-on PCI/ISA IDE card to be selected. This item is set at “Auto” for both the Optimal and Fail-Safe default settings.
- **IRQ3/4/5/7/10/11/15**

Available	Specified IRQ is available for use by PCI / PnP devices.
Reserved	Specified IRQ is reserved for use by Legacy ISA devices.

4.2.4 Boot Setup Utility

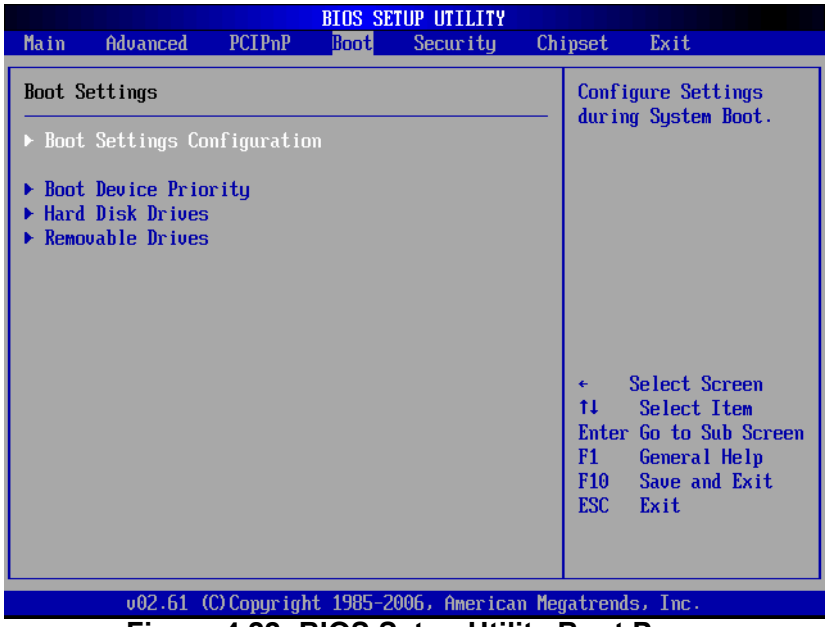


Figure 4.22: BIOS Setup Utility Boot Page

Note! *At least one HDD must be connected to ITA-2210 for the “Hard Disk Drives” option to be displayed in the BIOS setup screen.*

4.2.4.1 Boot Settings Configuration

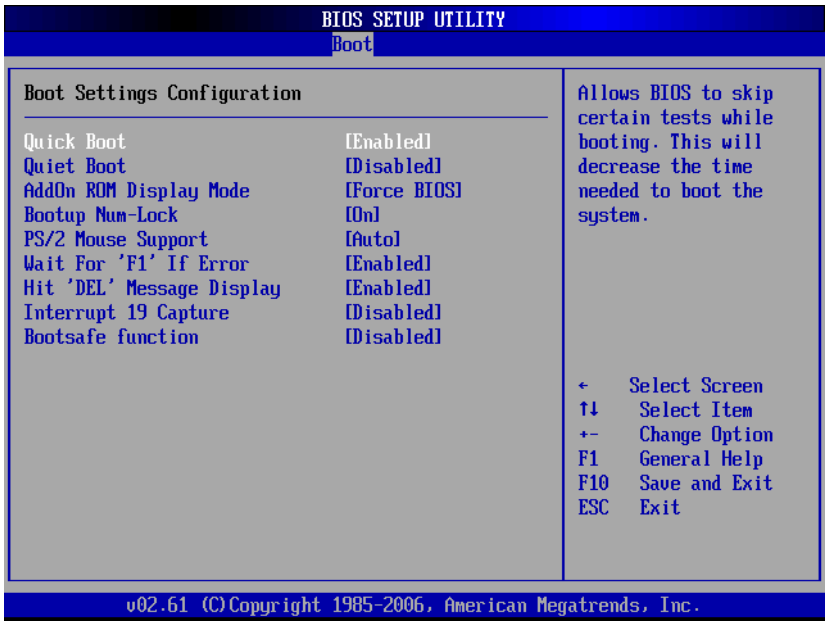


Figure 4.23: Boot Settings Configuration

- **Quick Boot**
  Allows the BIOS to skip certain tests when booting. The default setting is "Enabled".
- **Quiet Boot**
  If this option is set to "Disabled", the BIOS displays standard POST messages. If set to "Enabled", an OEM logo is displayed instead of POST messages.
- **AddON Rom Display Mode**
  Sets the display mode of optional ROM.
- **Bootup Num-Lock**
  Select the Power-On state for Numlock.
- **PS/2 Mouse Support**
  Select support for a PS/2 mouse (only available in DOS).
- **Wait For "F1" If Error**
  Commands the system to wait for the F1 key to be pressed if an error occurs.
- **Hit "Del" Message Display**
  Displays "Press Del to run Setup" in POST.
- **Interrupt 19 Capture**
  The ROM options for some add-on cards require Interrupt 19. This item allows users to enable or disable support for these types of add-on cards.This setting may be required for PCI cards depending on the ROM configuration utility.
- **Bootsafe Function**
  This item allows users to enable or disable the bootsafe function.

Boot Device Priority

This item allows users to configure the booting priority of the available devices, specifically, Hard Disk Device, Removable Device, and CD-DVD ROM.

4.2.5 Security Setup

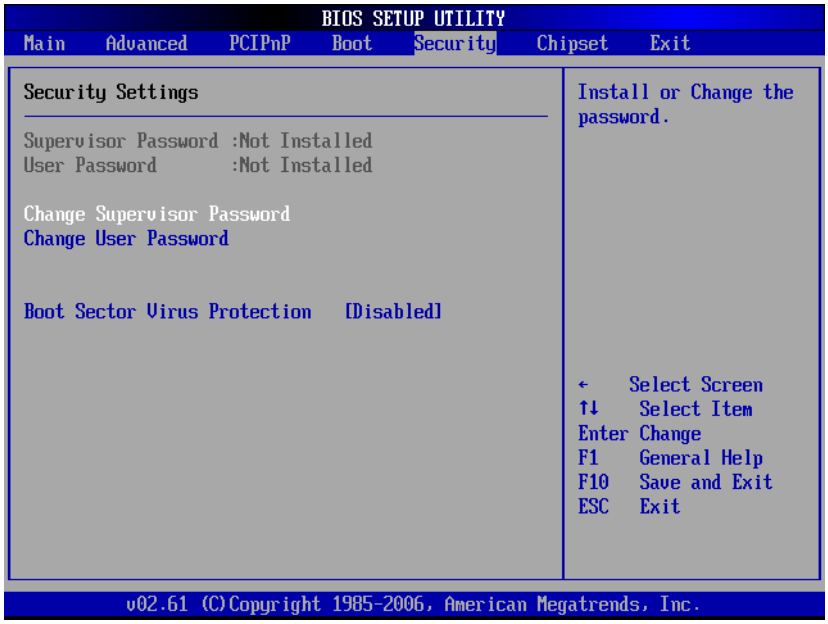


Figure 4.24: Password Configuration

Select the Security tab from the ITA-2210 BIOS Setup Utility menu. All Security options, such as Password Protection and Virus Protection, are described in this section. To access the submenu for the following items, select the item and press <Enter>:

- **Change administrator password**
- **Change user password**
- **Boot sector virus protection**

  The boot sector virus protection will display a warning if any program attempts to write to the boot sector. The default setting in DOS is “Disabled”.

4.2.6 Advanced Chipset Settings

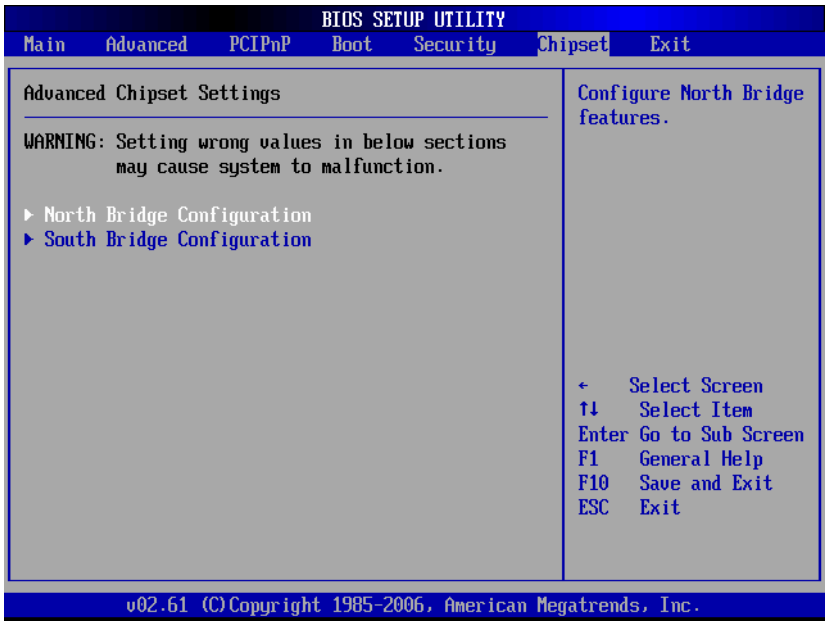


Figure 4.25: Advanced Chipset Settings

4.2.6.1 North Bridge Chipset Configuration

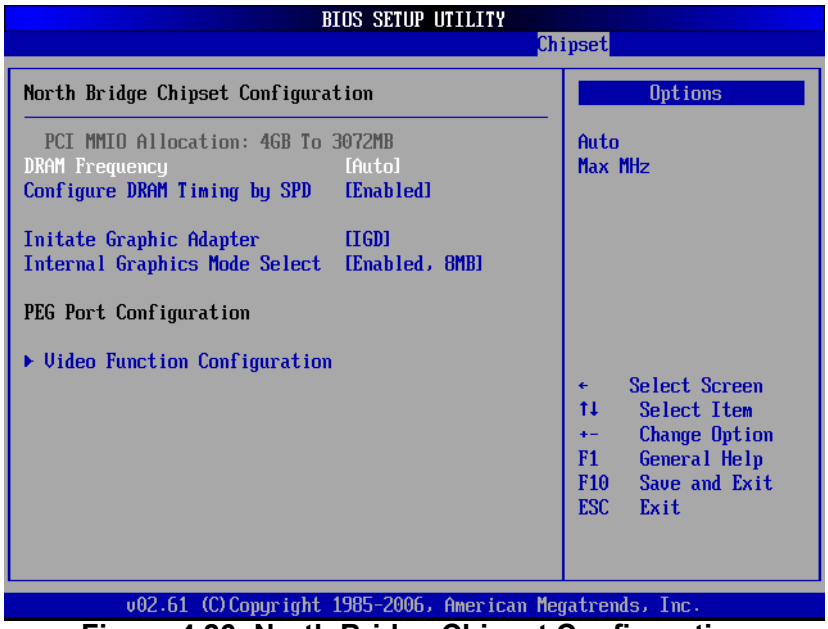


Figure 4.26: North Bridge Chipset Configuration

- **DRAM Frequency**

  This item allows users to select the DRAM frequency. The default setting is "Auto" using the serial presence detect (SPD) function.

- **Configure DRAM Timing by SPD**

  This item allows users to specify DRAM timing either by SPD or manually, and to enable or disable the DRAM SPD function.

- **Initiate Graphics Adapter**

  This item allows users to set the graphics controller used as the primary graphics device when booting up. Users are advised not to modify the item settings.

- **Internal Graphics Mode Select**

  This item allows users to allocate a portion of the system memory to the built-in graphics card.

- **Video Function Configuration**

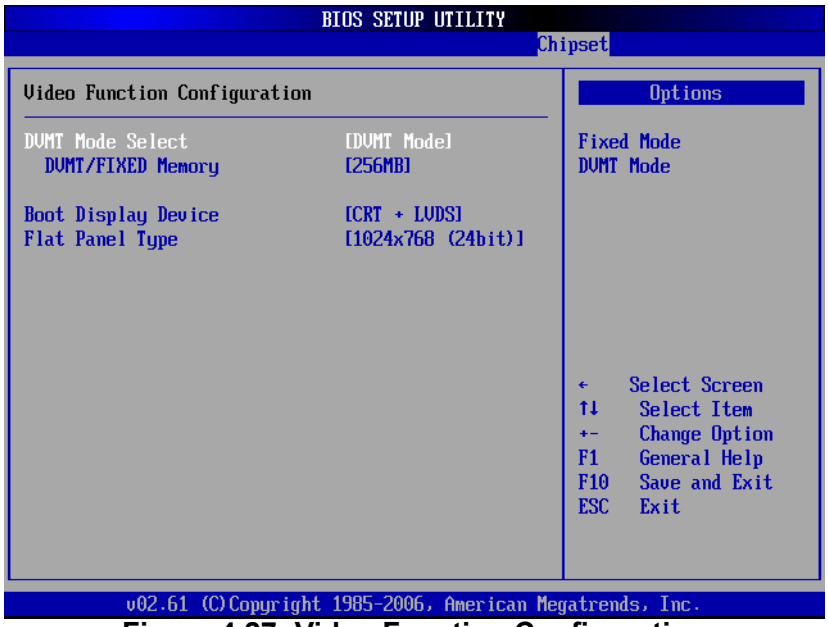


Figure 4.27: Video Function Configuration

  - **DVMT Mode Select**

    This item allows users to set the system video mode as either “DVMT mode” or “fixed mode”.

  - **DVMT / Fixed Memory**

    This item allows users to set the memory capacity for videos in “fixed mode”.

  - **Boot Display Device**

    This item allows users to specify the boot display device during the POST process. The default setting is “CRT+ LVDS”.

  - **Flat Panel Type**

    This item allows users to set the flat-panel display resolution. The default setting is “1024 x 768 (24 bit)”.

4.2.6.2 South Bridge Chipset Configuration

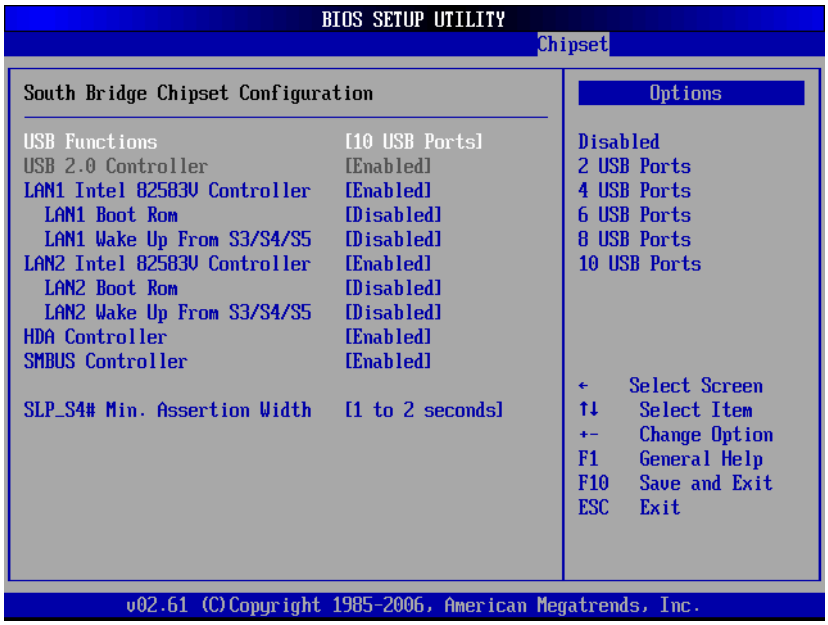


Figure 4.28: South Bridge Chipset Configuration

- **USB Functions**
  The default setting is “10 USB ports”.
- **USB 2.0 Controller**
  This item allows users to enable or disable the USB 2.0 controller. When USB Functions is set to “10 ports”, this option cannot be configured.
- **LAN1 Intel® 82583V Controller**
  This item allows users to enable or disable the Intel® LAN1 controller.
- **LAN1 Boot ROM**
  This item allows users to set the system to boot from “PCI ROM” or “Not for LAN1”.
- **LAN1 Wake Up from S3 / S4 / S5**
  This item allows users to enable or disable LAN1 wake up from S3 / S4 / S5.
- **LAN2 Intel® 82583V Controller**
  This item allows users to enable or disable the Intel® LAN2 controller.
- **LAN2 Boot ROM**
  This item allows users to set the system to boot from “PCI ROM” or “Not for LAN2”.
- **LAN2 Wake Up From S3 / S4 / S5**
  This item allows users to enable or disable LAN2 wake up from S3 / S4 / S5.
- **HDA Controller**
  This item allows users to enable or disable the HD audio controller.
- **SMBUS Controller**
  This item allows users to enable or disable the SMBus controller.
- **SLP_S4# Min. Assertion Width**
  This item allows users to set the minimum assertion width of Slp_S4# when booting up. The default setting is “1 - 2 seconds”.

4.2.7 Exit Options

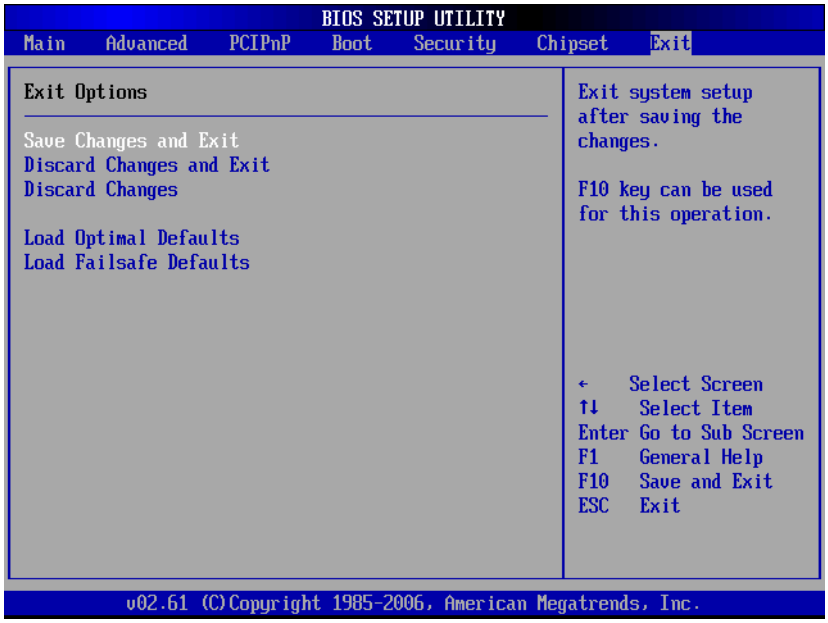


Figure 4.29: Exit Options

4.2.7.1 Save Changes and Exit

After completing the system configuration, select this option to save changes and exit the BIOS setup menu. Next, reboot the computer to implement the new system configuration parameters.

1. Select the “Save Changes and Exit” option from the Exit menu and press <Enter>. This should generate the following message:
   Save Configuration Changes and Exit Now?
   [OK] [Cancel]
2. Select “OK” or “Cancel”.

4.2.7.2 Discard Changes and Exit

Select this option to exit the BIOS setup menu without making permanent changes to the system configuration.

1. Select the “Discard Changes and Exit” option from the Exit menu and press <Enter>. This should generate the following message:
   Discard Changes and Exit Setup Now?
   [OK] [Cancel]
2. Select “OK” to discard changes and exit.

4.2.7.3 Discard Changes

Select the “Discard Changes” option from the Exit menu and press <Enter>.

4.2.7.4 Load Optimal Defaults

All setup options are automatically configured to their optimal settings when this function is enabled. Select the “Load Optimal Defaults” option from the Exit menu and press <Enter>.

4.2.7.5 Load Failsafe Defaults

All setup options are automatically configured to their fail-safe settings when this function is enabled. Fail-Safe defaults are designed for maximum system stability, not maximum performance. Select the “Fail-Safe Defaults” options from the Exit menu and press <Enter>.

Chapter 5

Driver Installation

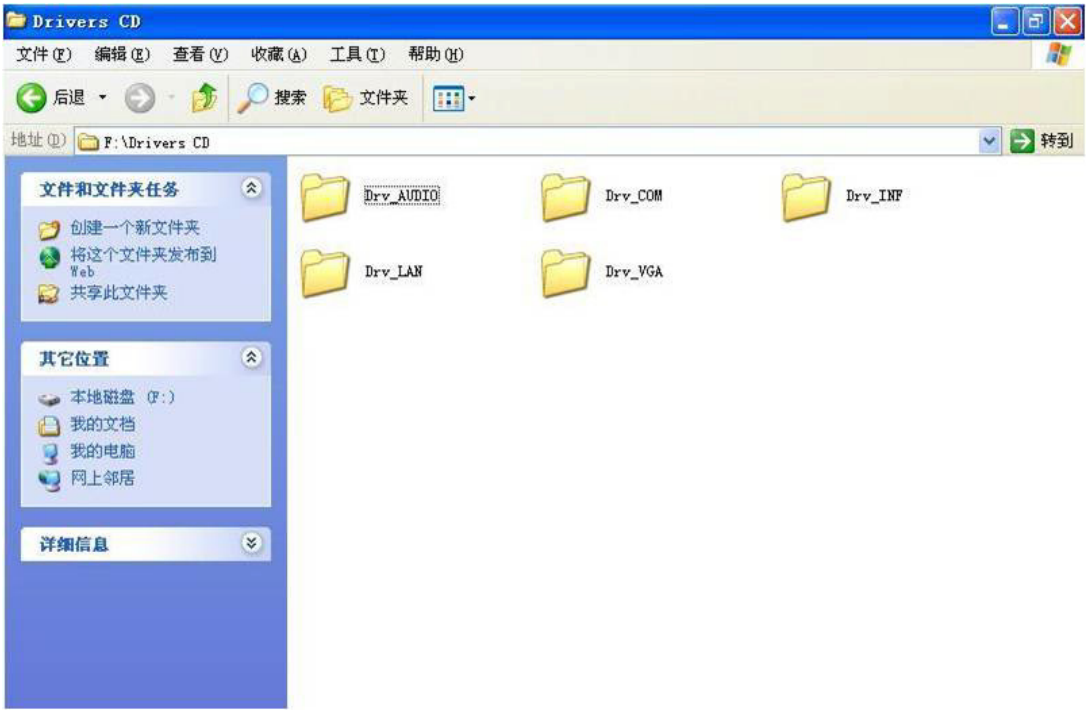
This chapter describes the driver installation process.

5.1 Introduction

Advantech offers a complete range of device drivers and software supports for Microsoft Windows programming developers. These Windows device drivers can be employed for most popular Windows programming tools, such as Visual C++, Visual Basic, Borland C++ Builder, and Borland Delphi.

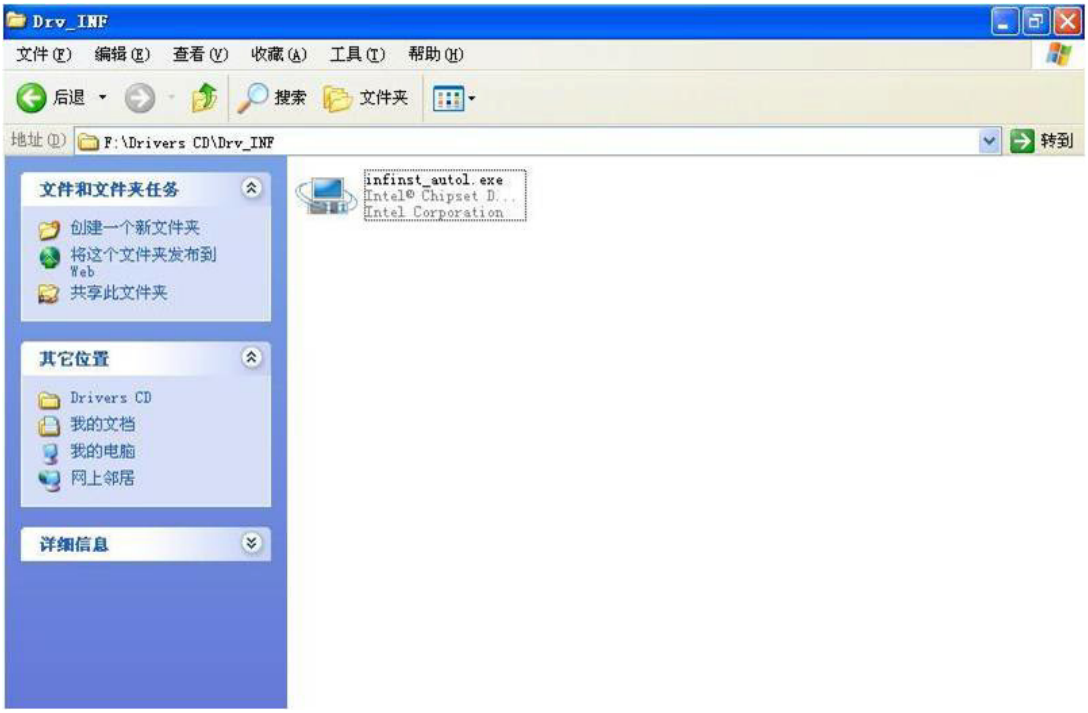
5.2 Driver Installation

Insert the driver CD in the system CD-ROM drive. The image below shows the folders included in the ITA-2210 drivers CD.



5.2.1 Chipset Windows Driver Setup

Insert the driver CD into the system CD-ROM drive to access the driver folder items. Navigate to the “Drv_INF” folder and click “infinst_autol.exe” to initiate driver installation.

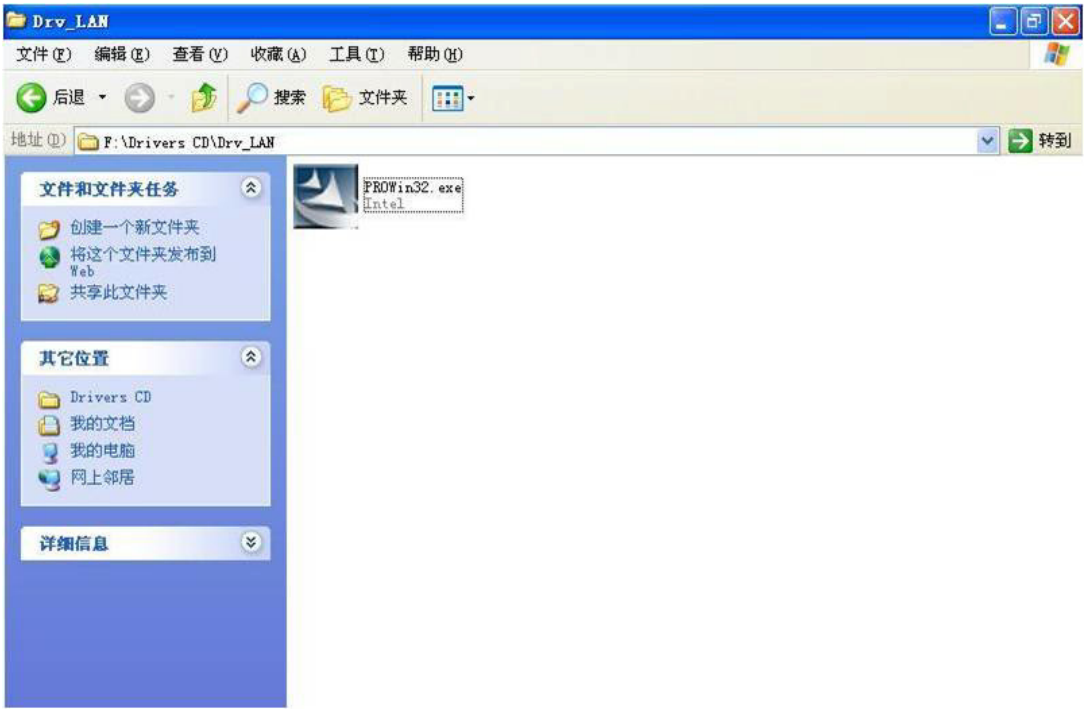


5.2.2 VGA Windows Driver Setup

Insert the driver CD into the system CD-ROM drive to access the driver folder items. Navigate to the “Drv_VGA” folder and click “Setup.exe” to initiate driver installation.

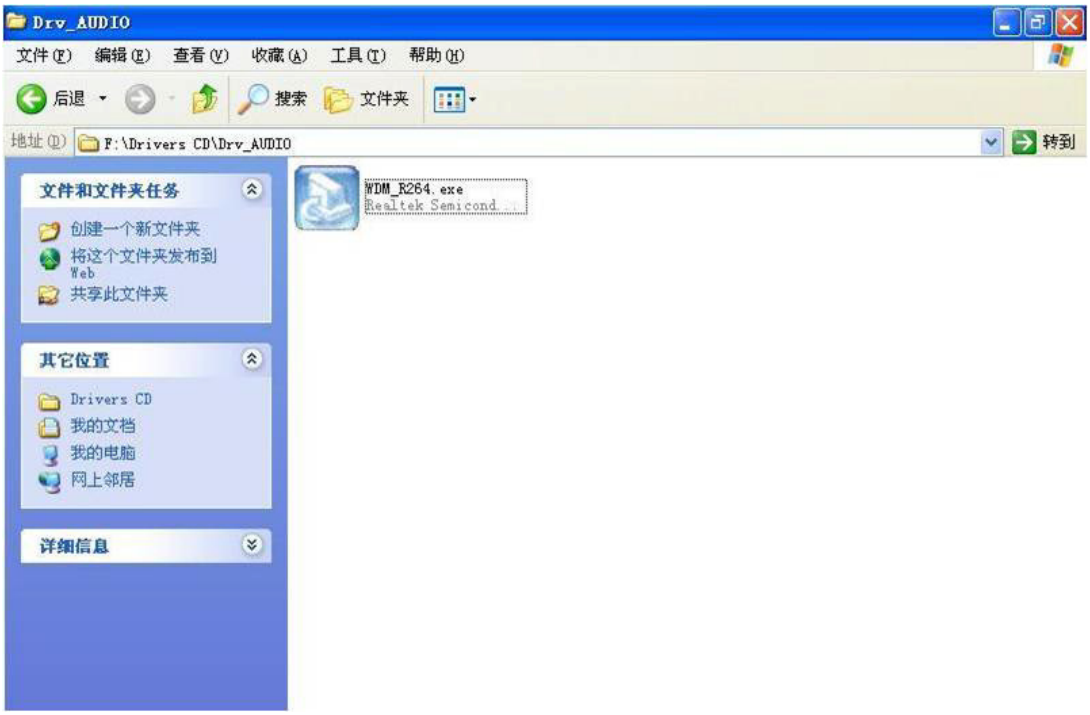
5.2.3 LAN Windows Driver Setup

Insert the driver CD into the system CD-ROM drive to access the driver folder items. Navigate to the “Drv_LAN” folder and click “PROWin32.exe” to initiate driver installation.



5.2.4 Audio Windows Driver Installation

Insert the driver CD into the system CD-ROM drive to access the driver folder items. Navigate to the “Drv_AUDIO” folder and click “WDM_R246.exe” to initiate driver installation.



Chapter 6

GPIO Programming Guide

This chapter provides information regarding GPIO programming.

Please carefully read the following examples and source codes presented in bold.

Next, download the NXP Semiconductors PAC9554 specification to begin programming.

6.1 Digital IO Definition of ITA-2210 (See Section 2.3.6)

6.2 Configuration Sequence

The ITA-2210 GPIO is realized using a PCA9554 GPIO IC on ICH SMBus. Thus, the GPIO IC should be configured and access via IO Space using the ICH SMBus controller.
Data of the ICH SMBus IO Space is provided in the following table:

SMB_BASE + Offset	Mnemonic	Register Name	Default	Type
00h	HST_STS	Host Status	00h	R/WC, RO, R/WC (special)
02h	HST_CNT	Host Control	00h	R/W, WO
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W

As shown in the above table, for the ITA-2210 system, the IO address of **SMB_BASE** is 0 x 400.

Refer to Chapter 3 to obtain the detailed code for accessing SMBus IO.

The SMBus slave address of PCA9554 for GPIO 00 to GPIO 07 is 0 x 40 (8-bit address):

GPIO 00 - GPIO 07: PCA9554 0 x 40 (IO0 - IO7)

Data of the PCA9554 is provided in the table below.

Symbol	Pin			Description
	DIP16, SO16, SSOP16, TSSOP16	HVQFN16	SSOP20	
A0	1	15	6	address input 0
A1	2	16	7	address input 1
A2	3	1	9	address input 2
IO0	4	2	10	input/output 0
IO1	5	3	11	input/output 1
IO2	6	4	12	input/output 2
IO3	7	5	14	input/output 3
V_{SS}	8	6[1]	15	supply ground
IO4	9	7	16	input/output 4
IO5	10	8	17	input/output 5
IO6	11	9	19	input/output 6
IO7	12	10	20	input/output 7
$\overline{INT}$	13	11	1	interrupt output (open-drain)
SCL	14	12	2	serial clock line
SDA	15	13	4	serial data line
V_{DD}	16	14	5	supply voltage
n.c.	-	-	3, 8, 13, 18	not connected

The PCA9554 register is shown below.

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

The PCA9554 is equipped with four registers for controlling GPIO.

PCA9554 Register 0

6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally '1' when no external signal externally applied because of the internal pull-up resistors.

Table 4. Register 0 - Input Port register bit description

Bit	Symbol	Access	Value	Description
7	I7	read only	X	determined by externally applied logic level
6	I6	read only	X	
5	I5	read only	X	
4	I4	read only	X	
3	I3	read only	X	
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

If a certain GPIO pin is set as an input, the corresponding input value can be obtained from the corresponding bit of Register 0.

PCA9554 Register 1

This register reflects the level of outgoing logic for pins defined as outputs by Register 3. The bit value listed in this register does not correspond to the input pin. When reading this register, the flip-flop value that controls output will be returned, whereas the pin physical signal value will not be returned.

6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 5. Register 1 - Output Port register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	O7	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

If a certain GPIO pin is set as an output, the corresponding output value can be obtained from the corresponding bit of Register 1.

PCA9554 Register 2

6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Table 6. Register 2 - Polarity Inversion register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	inverts polarity of Input Port register data
6	N6	R/W	0*	0 = Input Port register data retained (default value)
5	N5	R/W	0*	1 = Input Port register data inverted
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

If a certain GPIO pin is set as an input, set the corresponding bit of Register 2 to control the input pin.

PCA9554 Register 3

6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD}.

Table 7. Register 3 - Configuration register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	configures the directions of the I/O pins
6	C6	R/W	1*	0 = corresponding port pin enabled as an output
5	C5	R/W	1*	1 = corresponding port pin configured as input (default value)
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

Register 3 is used to set the GPIO as an input or output as follows:

If the corresponding bit is “0”, then the GPIO pin is set as “Output”.

If the corresponding bit is “1”, then the GPIO pin is set as “Input”.

Examples

Using the ITA-2210 system for this following example, assuming that GPIO 00 is set as “Output”, “GPIO 07” is set as “Input”, and both pins are connected, then the corresponding registers should be set as follows:

GPIO 00 corresponds to PCA9554 0 x 40 IO0, whereas GPIO 07 corresponds to PCA9554 0 x 40 IO7.

Set GPIO 00 as “Output”.

1. Read the value of the SMBus slave 0 x 40 Register 3 byte.
2. Set the bit 0 value obtained in Step 1 as 0 and write it to the SMBus slave 0 x 40 Register 3.
3. Read the value of the SMBus slave 0 x 40 Register 1 byte.
4. Depending on whether the output value is low or high, set the bit 0 value obtained in Step 3 as 0 or 1 and write it to the SMBus slave 0 x 40 Register 1.

Set GPIO 07 as “Input”.

1. Read the value of the SMBus slave 0 x 40 Register 3 byte,
2. Set the bit 7 value obtained in Step 1 as 1 and write it to the SMBus slave 0 x 40 Register 3,
3. Read the value of the SMBus slave 0 x 40 Register 0 byte,
   Determine whether the input value is low or high according to the value of bit 7 obtain in Step 3.

6.3 Function Call Reference

ICH SMBus Access Codes

The following codes simulate the BIOS on SMBus. Borand C++ 3.1 is suitable for compilation. These codes have been tested in DOS, but not on other operating systems.

```
#define SMBUS_PORT 0x400//SMB_BASE is 0x400
typedef  unsigned char BYTE;

////////////////////////////////////////////////////////////////////////////////////////////////
BYTE    smbus_read_byte(BYTE addr, BYTE offset)
//Read value of SMBus Register byte. One byte value is returned each time, among which addr is slave address, like 0x40; offset is register offset
{
        int     i;
        BYTE data;

        outportb(SMBUS_PORT + 4, (addr | 1));//Write slave address to SMB_BASE + 4 (Before reading, please set slave address bit 0 to 1, so there is addr|1)
        newiodelay();//delay
        newiodelay();//delay

        chk_smbus_ready();//Determine if SMBus is ready
```

```
        outportb(SMBUS_PORT + 3, offset);//Write register offset to SMB_BASE +
3
    newiodelay();//delay
        newiodelay();//delay

        outportb(SMBUS_PORT + 2, 0x48);//Write SBMBUS command
toSMB_BASE + 2, 0x48 means starting Byte data transmission
        newiodelay();//delay
        newiodelay();//delay

        for (i = 0; i <= 0x100; i++)
        {
            newiodelay();//long time delay
        }

        chk_smbus_ready();//Determine if SMBus is ready
        return(inportb(SMBUS_PORT + 5));//Read byte value from SMB_BASE + 5
}

////////////////////////////////////////////////////////////////////////////////////////////
void    smbus_write_byte(BYTE addr, BYTE offset, BYTE value)
//Write SMBus Register byte value. One byte value can be written each time, among
which addr indicates slave address, like 0x40; offset is register offset; value is the
value to be written
{
        int     i;

        outportb(SMBUS_PORT + 4, addr);//Write slave address to SMB_BASE + 4
(Please set slave address bit 0 to 0 before writing)
        moredelay();//long time delay
        moredelay();//long time delay

        chk_smbus_ready();//Determine if SMBus is ready

        outportb(SMBUS_PORT + 3, offset);//write register offset to SMB_BASE + 3
        moredelay();//long time delay
        moredelay();//long time delay

        outportb(SMBUS_PORT + 5, value);//Write data value to SMB_BASE + 5
        moredelay();//long time delay
        moredelay();//long time delay

        outportb(SMBUS_PORT + 2, 0x48);//Write SMBus command to
SMB_BASE + 2, 0x48 means starting Byte data transmission
        moredelay();//long time delay
        moredelay();//long time delay
```

```
        for (i = 0; i <= 0x100; i++)
        {
                newiodelay();//long time delay
        }

        chk_smbus_ready();//Determine if SMBus is ready
}

////////////////////////////////////////////////////////////////////////////////////////////////
int     chk_smbus_ready()
//Determine if SMBus is ready or finished. Basically, it will wait for a long time to see whether SMBus has finished the transmission command because errors hardly occur. So, in SMBus byte read and write, BIOS Code does not determine the return value of this function
{
        int     i, result = 1;
        BYTE data;

        for (i = 0; i <= 0x800; i++)
        {
                //SMB_BASE + 0 is SMBus status value
                data = inportb(SMBUS_PORT);//Read SMBus status value once
                data = check_data(SMBUS_PORT);//Read SMBus status value several times
                outportb(SMBUS_PORT, data);//Write back SMBus status value which means clear status value(Write 1 to the corresponding bit will clear status)

                if (data & 0x02)
                {       //If bit 1 is set to 1 (this means the command is finished), then SMBus is ready
                        result = 0;//SMBus ready
                        break;
                }

                if (!(data & 0xBF))
                {       //If each bit except bit 2 is set to 0, this means SMBus error , then SMBus is ready
                        result = 0;//SMBus ready
                        break;
                }

                if (data & 0x04)
                {       //If bit 2 is set to 1 (this means SMBus error), then error has occurred in SMBus. This rarely happens
                        result = 1;//SMBus error
                        break;
                }
```

```
        }

        returnresult;
}

////////////////////////////////////////////////////////////////////////////////////////////////
BYTE    check_data(WORD addr)
{
        int     i;
        BYTE data;

        for(i = 0; i <= 6; i++)
        {
                data = inportb(addr);
                if (data != 0)
                        break;
        }

        returndata;
}

////////////////////////////////////////////////////////////////////////////////////////////////
void    newiodelay()
//shot time delay
{
        outportb(0xeb, 0);//IO port 0xeb is not occupied by any device actually. Writ-
ing value to this port can cause time delay. The user can also use other methods
instead
}
////////////////////////////////////////////////////////////////////////////////////////////////
void    moredelay()
//long time delay
{
        int     i;
        for (i = 0; i < 20; i++)
        {
                outportb(0xeb, 0);//IO port 0xeb is not occupied by any device actually.
Writing value to this port can cause time delay. The user can also use other methods
instead
        }
}

**************************************************************************
GPIO simulation code
(Take GPIO 00 and GPIO 07 in Chapter 2 for example)
```

GPIO 00 output High:

```
data = smbus_read_byte(0x40, 0x03);//Read slave 0x40 register 3 byte
data &= 0xfe;//Set bit 0 to 0
smbus_write_byte(0x40, 0x03, data)//Write back, GPIO 00 is set to Output
data = smbus_read_byte(0x40, 0x01)//Read slave 0x40 register 1
data |= 0x01;//Set bit 0 to 1, which means High
smbus_write_byte(0x40, 0x01, data)//Write back, output High value
```

Read Input value from GPIO 07:

```
data = smbus_read_byte(0x40, 0x03);//Read slave 0x40 register 3 byte
data |= 0x80;//Set bit 7 to 1
smbus_write_byte(0x40, 0x03, data)//Write back,GPIO 07 is set to Input
data = smbus_read_byte(0x40, 0x00)//Read slave 0x40 register 0.
```

Response value of bit 7 can determine whether Input is Low or High

Appendix A

Programming the Watchdog Timer

A.1 Programming the Watchdog Timer

The ITA-2210's watchdog timer can be used to monitor the system software operation and execute corrective action should the software fail to function within a set period. The operation and programming of the watchdog timer is explained in this section.

A.1.1 Watchdog Timer Overview

The watchdog timer is built into the SMSC SCH3114super I/O controller and has the following programmable functions:

- Can be enabled or disabled via a user program
- The timer can be set to 1 ~ 255 seconds or 1 ~ 255 minutes
- Generates an interrupt or reset signal if the software fails to reset the timer before the timeout value is reached

A.1.2 Programming the Watchdog Timer

The I/O port address of the watchdog timer is B00h (hex).

Table A.1: Watchdog Timer Registers

Address: B00h (hex)

Register Shift	Read / Write	Description
65 (hex)	Write	Set the timer unit to be either seconds or minutes. Write 0 to bit 7: set the unit of measure as seconds (default). Write 1 to bit 7: set the unit of measure as minutes.
66 (hex)	Write	0: Stop timer (default) 01~ FF (hex): The unit value, in seconds or minutes, depends on the value set in Register 65 (hex). This value determines the duration of time the watchdog timer waits for strobe before generating an interrupt or reset signal. Writing a new value to this register resets the timer to being counting from the new value.
67 (hex)	Read / Write	Configure the watchdog timer Bit 1: Write 1 to enable the keyboard to reset the timer, and 0 to disable (default). Bit 2: Write 1 to enable the mouse to reset the timer, and 0 to disable (default). Bit 7 ~ 4: Set the interrupt mapping of the watchdog timer: 1111 = IRQ15 …… 0011 = IRQ3 0010 = IRQ2 0001 = IRQ1 0000 = Disable (default)
68 (hex)	Read / Write	Control the watchdog timer Bit 0: Read the watchdog state; 1 = Timer timeout reached Bit 2: Write 1 to immediately generate a timeout signal, and automatically return to 0 (write only). Bit 3: Write 1 to allow the triggering of timer timeout when P20 is effective, and 0 to disable (default).

A.1.3 Example Program

1. Enable the watchdog timer and set the timeout interval to 10 seconds.

```
Mov dx, A65h; select Register 65h, watchdog timer I/O port address B00h+ register shifts 65h
Mov al,80h; set the unit of measure as seconds
Out dx,al

Mov dx,A66h; select Register 66h, watchdog timer I/O port address B00h+ register shift 66h
Mov al10; set the timeout interval to 10 seconds and start counting
Out dx,al
;-------------------------------------------------------
```

2. Enable the watchdog timer and set the timeout interval to 5 minutes

```
;-------------------------------------------------------
Mov dx,A65h; select Register 65h, watchdog timer I/O port address B00h+ register shifts 65h
Mov al,00h; set the unit of measure as minutes
Out dx,al

Mov dx,A66h; select Register 66h, watchdog timer I/O port address B00h+ register shifts 66h
Mov al,5; set the timeout interval to 5 minutes and start counting
Out dx,al
;-------------------------------------------------------
```

3. Enable the watchdog timer to be reset using the mouse

```
;-------------------------------------------------------
Mov dx,A67h; select Register 67h, watchdog timer I/O port address B00h+ register shifts 67h
In al,dx
Or al,4h; enable the watchdog timer to be reset using the mouse
Out dx,al
;-------------------------------------------------------
```

4. Enable the watchdog timer to be reset using the keyboard

```
;-------------------------------------------------------
Mov dx,A67h; select Register 67h, watchdog timer I/O port address B00h+ register shifts 67h
In al,dx
Or al,2h; enable the watchdog timer to be reset using the keyboard
Out dx,al
;-------------------------------------------------------
```

5. Generate a timeout signal without the timer counting

```
;-------------------------------------------------------
Mov dx,A68h; select Register 68h, watchdog timer I/O port address B00h+ register shifts 68h
In al,dx
Or al,4h; generate a timeout signal
Out dx,al
;-------------------------------------------------------
```

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