

User Manual

MIC-5332

**AdvancedTCA® 10GbE Dual Socket CPU Blade
with Intel® Xeon® E5-2600 series EP Processors**

Revision History

Revision Index	Brief Description of Changes	Date of Issue
0.1	Initial Draft	November 15 th , 2011
0.2	Modification	April 11 th , 2012
0.3	Modification	June 15 th , 2012
0.4	Modification	July 16 th , 2012

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5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his or her own expense.

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1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
 - ◆ Product name and serial number
 - ◆ Description of your peripheral attachments
 - ◆ Description of your firmware version
 - ◆ A complete description of the problem
 - ◆ The exact wording of any error messages

Warnings, Cautions and Notes

Warning! Warnings indicate conditions, which if not observed, can cause personal injury.



Caution! Cautions are included to help you avoid damaging hardware or losing data, for example, there is a danger of a new battery exploding if it is incorrectly installed.

Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer.

Discard used batteries according to the manufacturer's instructions.



Note! Notes provide optional additional information.



Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing to: support@advantech.com

Packing List

- ◆ RJ45 to DB9 Console Cable x1, p/n: 1700002270
- ◆ Mini-USB to USB Console Cable x1, p/n: 1700018550
- ◆ Warranty certificate document x, p/n: 2190000902

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Keep this equipment away from humidity.
4. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
5. All cautions and warnings on the equipment should be noted.
6. Always use caution when handling/operating the computer. Only qualified, experienced, authorized electronics service personnel should access the interior of the computer. Te power supplies produce high voltages and energy hazards, which can cause bodily harm.
7. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient over-voltage.
8. Never pour any liquid into an opening. This may cause fire or electrical shock.
9. If one of the following situations arises, get the equipment checked by service personnel:
 - The power cord or plug is damaged.
 - Liquid has penetrated into the equipment.
 - The equipment has been exposed to moisture.
 - The equipment does not work well, or you cannot get it to work according
 - The equipment has been dropped and damaged.
 - The equipment has obvious signs of breakage.
10. The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from your system chassis before you work on it. Don't touch any components on the CPU card or other cards while the system is on.
2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.
3. When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the omponent in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
4. When transporting a sensitive component, first place it in an antistatic container or packaging.

We Appreciate Your Input

Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

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Glossary

ACPI	Advanced Configuration and Power Interface
AHCI	Advanced Host Controller Interface
AMC	Advanced Mezzanine Card
APIC	Advanced Programmable Interrupt Controller
ATCA	Advanced Telecommunications Computing Architecture
BI	Base Interface
BMC	Baseboard Management Controller
CMC	Carrier Management Controller
EHCI	Enhanced Host Controller Interface
FI	Fabric Interface
FMM	Fabric Mezzanine Module
FRU	Field Replaceable Unit
FW	Firmware
GbE	Gigabit Ethernet
HPM	Hardware Platform Management
IOH	I/O Controller Hub
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
MCH	Memory Controller Hub
NVRAM	Non-volatile Random Access Memory
OOS	Out Of Service
PCH	Platform Controllers Hub
PCIe	PCI Express
PECI	Platform Environment Control Interface
PICMG	PCI Industrial Computer Manufacturers Group
PXE	Pre-boot Execution Environment
QPI	QuickPath Interconnection
RDIMM	Registered DIMMs
RMCP	Remote Management Control Protocol
RTM	Rear Transition Module
RX	Receive
SAS	Serial Attached SCSI
SATA	Serial Advanced Technology Attachment
SCSI	Small Computer System Interface
SDR	Sensor Data Record
SerDes	Serializer/Deserializer

ShMC	Shelf Manager Controller
SOL	Serial Over LAN
TCLK	Telecom Clock
TPM	Trusted Platform Module
TX	Transmit
UDIMM	Unbuffered DIMMs
UHCI	Universal Host Controller Interface
VLP	Very Low Profile
XAUI	X (means ten) Attachment Unit Interface

Chapter 1

Product Overview

This chapter briefly describes the MIC-5332.

1.1 MIC-5332 Overview

The MIC-5332 is a dual socket AdvancedTCA blade based on the Intel® Xeon E5-2600 series EP processors and C600 PCH (codename Patsburg). The MIC-5332 enables the highest performance available in an ATCA form factor with up to 16-cores and 32-threads of processing power, fast PCI Express gen 3 lanes running at up to 8Gbps, and best in class virtualization support. Two QPI interfaces between the CPUs improve memory and I/O access throughput and latencies when one processor needs to access resources hosted by the other socket. With four DDR3 DIMMs per socket in a quad channel design running up to 1600MT/s, the MIC-5332 not only offers superior memory bandwidth over 3-channel designs, but can also support memory densities up to 256GB using latest LR DIMM technology. It outperforms previous generation dual socket designs while keeping similar thermal characteristics with balanced airflow resistance.

Using Intel's latest PCH (C604) with its integrated 4-port SAS controller, the need for an external storage controller is eliminated, making the MIC-5332 an ideal choice for cost sensitive control plane applications. While supporting two 10GBaseKX4 interfaces in the base model, support for dual-dual star fabric implementations can be added by installing the FMM-5001B Fabric Mezzanine Module (FMM). Beyond that, the FMM type II socket with PCIe x16 connectivity provides extension possibilities for additional front port I/O, offload and acceleration controllers such as Intel QuickAssist™ accelerators, IPSec offload engines or customer specific logic. FMMs not only have higher PCI Express bandwidth than AMCs, but also integrate well in terms of thermal design and board real estate when compared to Advanced Mezzanine Cards. Moreover, FMMs can be reused on RTMs and across different blade designs. This unmatched flexibility combined with the highest performance Intel® Xeon® processors available make the MIC-5332 equally well suited for application and data plane workloads.

The onboard IPMI firmware was developed entirely by Advantech to offer greater modularity and flexibility for the customization of system management features, especially when it comes to tailoring a system design to meet target cost points without sacrificing features and time to market. HPM.1 based updates are available for all programmable components (BIOS, IPMC firmware, FPGA) including rollback support. Advantech's IPMI solution, combined with an optimized AMI UEFI BIOS continues to offer advanced features used on previous generation MIC-532x blades, such as BIOS redundancy, Real Time Clock Synchronization, and MAC

Mirroring.(please refer to chapter 4) Advantech IPMI firmware has been tested for CP-TA compliance using the Polaris Networks ATCA Test Suite.

The MIC-5332 supports hot-swappable RTMs such as the RTM-5104 for High Availability (HA) needs, rear I/O and dual SAS storage with RAID as well as an optional FMM. Please contact Advantech for more information on available RTMs.

An on-board FPGA design facilitates customer-specific modifications, and the core board design can be modified or adapted to other form factors through Advantech's DMS customization services.

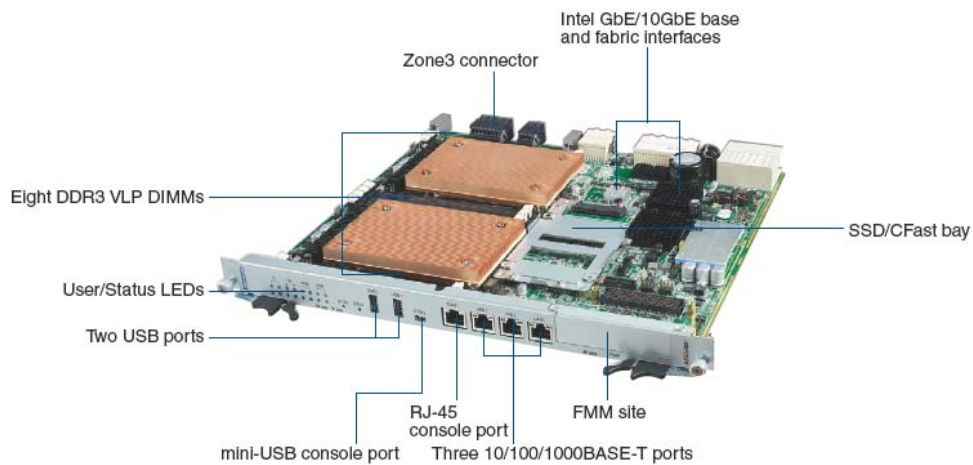
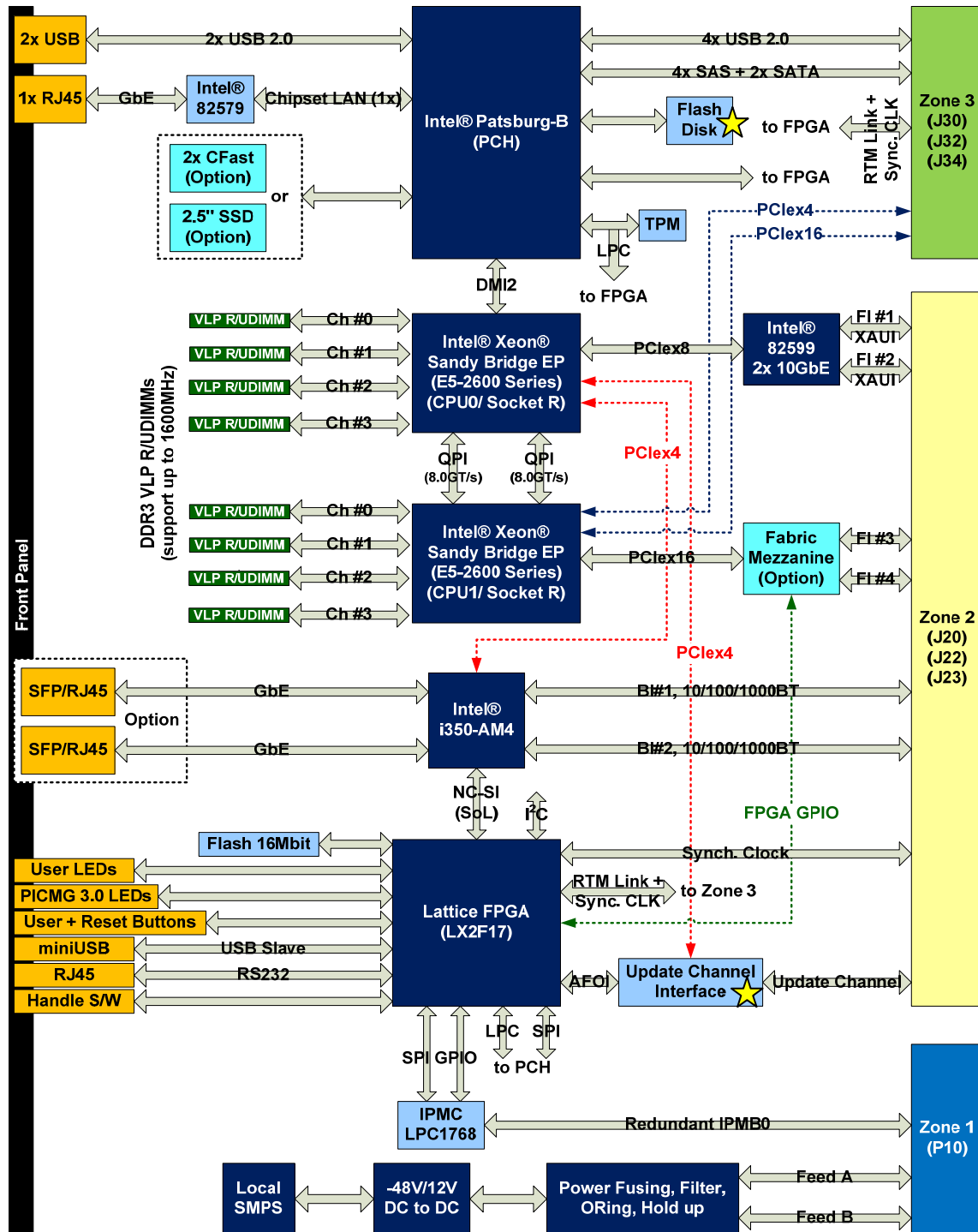


Figure 1.1 MIC-5332 Overview (Top Side)

1.2 Block Diagram

The hardware implementation is shown in the following block diagram. Refer to Table 1.1 (next page) for the detailed product technical specification.



★ : Option

Figure 1.2 MIC-5332 Block Diagram

1.3 Product Configurations

Model Name	Configurations
MIC-5332SA1-P1E	MIC-5332 RJ45 version with dual Intel® Xeon® E5-2648L CPU
MIC-5332SA1-P2E	MIC-5332 RJ45 version with dual Intel® Xeon® E5-2658 CPU
MIC-5332SB1-P1E	MIC-5332 SFP version with dual Intel® Xeon® E5-2648L CPU
MIC-5332SB1-P2E	MIC-5332 SFP version with dual Intel® Xeon® E5-2658 CPU

Table 1.1 MIC-5332 Configurations



Note:

- ◆ Support max 256GB using 8 pieces of 32GB DDR3-1600 VLP DIMM modules.

1.4 Related Products

Model Name	Configurations
RTM-5104	I/O extension ATCA RTM for MIC-5332
FMM-5001BE	Dual 10GE Module with 2x fabric ports for dual dual star support based on i82599EB
FMM-5001FE	Dual 10GE Module with 2x SFP+ front IO based on i82599ES
FMM-5002E	Server Graphics Module with external VGA Port
FMM-5006E	MIC-5332 QuickAssist Accelerator FMM

Table 1.2 MIC-5332 Related Products



Note:

- ◆ Contact Advantech for information on available and future RTMs and FMMs.

Chapter 2

Board Features

This chapter describes the MIC-5332 hardware features.

2.1 Technical Data

Processor System	CPU	Dual Intel® Xeon® E5-2648L/E5-2658 8-core processors ⁽¹⁾
	Max. Speed	2.1GHz
	Chipset	Intel® C604
	BIOS	Dual 64-Mbit BIOS firmware flashes with AMI UEFI based BIOS
	QPI	8.0 GT/s
Memory	Technology	Four channel DDR3 1066/1333/1600MHz SDRAM (72-bit ECC Un-/Registered), LR DIMM support
	Max. Capacity	Configurable up to 256 GB
	Socket	8 VLP DIMMs
Zone 2	Fabric interface	2 x Intel® 82599 Dual 10GE MAC/PHY supporting four 10GBase ports (XAUI) (one by default and the second one is optional, via a FMM-5001BE)
	Base interface	i350 GbE MAC/PHY supporting two 10/100/1000Mbps ports
Front I/O Interface	Serial (COM)	2 x 16C550 compatible Serial Ports (1 RJ-45 connector, 1 connector)
	Ethernet	2 x 10/100/1000BASE-T or SFP through i350 MAC/PHY, 1x 10/100/1000 BASE-T Chipset LAN
	USB 2.0	2 x Type A ports
Operating System	Compatibility	WindRiver PNE/LE 4.2, RedHat Enterprise 5.7 & 6.2, CentOS 6.1, Windows Server 2008
IPMC	BMC Controller	NXP LPC1768 (Cortex M)
	IPMI	Compliant with IPMI 1.5 using Advantech IPMI code base
Watchdog Timer	Supervision	1 for x86 BIOS POST, OS Boot, Application
	Interval	IPMI compliant
FMM	Site	1 FMM type II socket
	Interface	1 x PCIe x16 or 2 x PCIe x8
Miscellaneous	Storage	2 x CFast / 1 x 2.5" SSD*, , 4-port SAS controller integrated in PCH to zone 3
	Real Time Clock	Built-in
Power Requirement	Configuration	2 x E5-2648L70W, 32GB memory, no FMM, no RTM
	Consumption	230W (estimated)
Zone 3 (RTM)	RTM	Advantech common RTM interface Type 2
	Interface	4 x SAS/SATA, 1 x PCIe x16, 4 x USB, 2 x UART
Physical Characteristics	PCB Dimensions	6HP, 280.00 x 322.25 mm (11.02" x 12.69") (W x D)
	Weight	3.275kg

Environment		Operating	Non-operating
	Temperature	0 ~ 55° C (32 ~ 131° F)	- 40 ~ 70° C (-40 ~ 158° F)
	Humidity	5 to 93%@40°C (non condensing)	95% @ 40° C (non-condensing)
	Shock	4 G each axis	20 G each axis
	Vibration (5~500Hz)	0.5 Grms	2.16 Grms, 30 mins each axis
Compliance	Environment	ETSI EN300019-2-1 Class1.2, EN300019-2-2 Class 2.3, ETSI EN300019-2-3 Class 3.1E, Designed to meet GR63-CORE	
	PICMG	3.0 R3.0, 3.1 R1.0, HPM.1	
	Safety	CE mark (EN60950-2001), UL60950-1/CSAC22.2	
	EMC	FCC47 CFR Part15, Class A, CE Mark (EN55022 / EN55024 / EN300386), Designed to meet GR1089-CORE	

Table 2.1 MIC-5332 Technical Data

- ◆  **Note:** MIC-5332 supports 2 x 95W CPUs. Special system airflow requirements apply.
- ◆ CFast and 2.5" SSD are mutually exclusive.

2.2 Product Features

2.2.1 Processors

The MIC-5332 supports dual Intel® Xeon® E5-2600 series processors, using latest 32nm silicon architectures with built-in memory controller. It is a two-chip platform (CPU and PCH) as opposed to traditional three-chip platforms (CPU, MCH and IOH).

The Intel® Xeon® E5-2600 series feature per socket, two Intel® QuickPath Interconnect point-to-point links capable of up to 8.0 GT/s, up to 40 lanes of Gen 3 PCI Express links capable of 8.0 GT/s, and 4 lanes of DMI2/PCI Express Gen 2 interface with a peak transfer rate of 5.0 GT/s. The processor supports up to 46 bits of physical address space and 48-bit of virtual address space. It is also capable to support up to 4 channels DDR3 DIMM, supports both to UDIMMs and RDIMMs (more details about DDR3 DIMM supported specification, please refer to section 2.3). The MIC-5332 currently supported processors are listed as table 2.2:

Model	Cores/Threads	Frequency	L3 cache	DDR3 support	TDP	Socket
Xeon E5-2620	6C/12T	2.00 GHz	15 MB	DDR3-1333	95 Watt	LGA2011
Xeon E5-2648L	8C/16T	1.80 GHz	20 MB	DDR3-1600	70 Watt	LGA2011
Xeon E5-2658	8C/16T	2.10 GHz	20 MB	DDR3-1600	95 Watt	LGA2011

Table 2.2 MIC-5332 Supported Processors List

The E5 series Xeon processors support cache memory as listed below:

- ◆ A 32-KB instruction and 32-KB data first-level cache (L1) for each core.
- ◆ A 256-KB shared instruction/data mid-level (L2) cache for each core.
- ◆ Up to 20 MB last level cache (LLC): up to 2.5 MB per core instruction/data last level cache (LLC), shared among all cores.

2.2.2 Platform Controller Hub (PCH)

An Intel® C604 provides the peripheral connection in the Intel® Sandy Bridge platform. It contains DMI Gen2, 8x PCIe Gen2 root ports, 2x SATA 6Gb/s, 4x SATA 3Gb/s, 4x SAS 3Gb/s, 14x USB 2.0 and supports one internal GbE MAC. For more details, please refer to section 2.3.

2.2.3 DMI Gen2

Direct Media Interface (DMI) is the chip-to-chip connection between the processor and PCH. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally. New for C604 chipset, the DMI interface operates at 5.0 GT/s.

2.2.4 PCI Express Port Configuration

Intel® Xeon® E5-2600 series processors support 40 PCI Express Gen3 ports. They are configured to two x16 ports, one x8 port and five x4 ports in the MIC-5332. The PCI Express interface is connected to RTM (Port1 and 2) and update channel (Port 3, optional).

CPU	Port No.	Width	Description
0	0	x4	Connection for DMI between the CPU and PCH
	1	x4	Base Interface and I/O Control, connected to Intel® i350-AM4
	2	x8	Fabric Interface, connected to Intel® i82599 10GbE controller
	3	x4	For update channel, connected to Zone 2 (optional)
1	0	x4	Not connected
	1	x4	For RTM use, connected to Zone 3
	2	x16	For RTM use, connected to Zone 3
	3	x16	connected to fabric mezzanine (FMM); configurable as 1x16 or 2x8

Table 2.3 PCI Express Port Configuration on the MIC-5332



Note:

- ◆ PCIe hot swap is not supported for graphic controllers (e.g. FMM-5002E) installed on a RTM.

2.2.5 Redundant BIOS Flash

The MIC-5332 has two SPI flash devices for storing redundant x86 firmware (BIOS, BIOS configuration, etc.). The integrated management controller (IPMC) controls which flash device is active. Failover and rollback operations between the flash devices are compliant to HPM.1. By default, the MIC-5332 starts to boot from the active BIOS chip and will switch to the backup BIOS chip if it detects a problem, i.e. the BIOS is stuck in POST or fails to boot. For more details, please refer to Chapter 5, about AMI BIOS setup. From OS side of view, there is only the active BIOS SPI flash visible at any time.

2.2.6 Serial ATA and Serial Attached SCSI Controller

The MIC-5332 supports a total of 6 SATA and 4 SAS lanes.

The built-in Serial ATA (SATA) and Serial Attached SCSI (SAS) controller in the Intel® C600 PCH has three modes of operation to support different operating system conditions. In the case of a Native IDE enabled operating system, the C600 PCH utilizes two controllers to enable all six ports of the bus. The first controller (Device 31: Function 2) supports ports 0-3 and the second controller (Device 31: Function 5) supports ports 4 and 5. When using a legacy operating system, only one controller (Device 31: Function 2) is available which supports ports 0-3. In AHCI or RAID mode, only one controller (Device 31: Function 2) is utilized, enabling all six ports and the second controller (Device 31: Function 5) will be disabled. Please contact your Advantech technical support team for more detail information.

In the MIC-5332, SATA 6 Gbps support is available on PCH Ports 0 and 1 only, and reserved for onboard storage modules like CFast or 2.5" SSD. For detailed configurations, please refer to table 2.4:

Port No.	Speed	Description
0	6Gbps	Onboard Storage Module, 1x 2.5" SSD (default) or 2x CFast (option)
1	6Gbps	
2	3Gbps	SATA devices on the RTM (connected to Zone 3)
3	3Gbps	
4	3Gbps	on board SATA NAND Flash (optional)
5	3Gbps	SATA devices on FMM (optional)

Table 2.4 SATA Port Configuration on the MIC-5332

The MIC-5332 is also able to support SAS devices. 4 SAS 2.0 channels are reserved for SAS or SATA devices on RTM boards. For details, please see table 2.5.

Port No.	Speed	Description
0	3Gbps	Supports extended SAS/SATA devices on RTM (connected to Zone 3)
1		
2		
3		

Table 2.5 SAS Port Configuration on the MIC-5332

2.2.7 USB Controller

In the Intel® C600 PCH there are 14x USB ports, controlled either through the standard Universal Host Controller Interface (UHCI) for full/low speed support, or through Enhanced Host Controller Interface (EHCI) for USB 2.0 high speed support. The USB port connection in the MIC-5332 is listed in table 2.6.

Port No.	Description
0-1	Front Panel Ports
2-3	USB devices on a FMM
4-7	Not used
8-11	USB devices on an RTM (connect to Zone 3)
12-13	Not used

Table 2.6 USB Ports C on the MIC-5332

2.2.8 Real-time Clock (RTC)

Because there is no battery assembled on the MIC-5332, the integrated real-time clock is fed by IPMC management power. Due to the on-board super cap, the date and time can be kept for up to 2 hour periods of power loss

2.3 DDR3 DIMMs

2.3.1 Memory Characteristics

The MIC-5332 uses DDR3 VLP SDRAM. As shown in Figure 2.2, each CPU uses 4 channels on the MIC-5332, and each channel supports one un-buffered/registered ECC VLP DIMM, for a total of 8 sockets. Supported memory characteristics on the

MIC-5332 are listed as table 2.7.

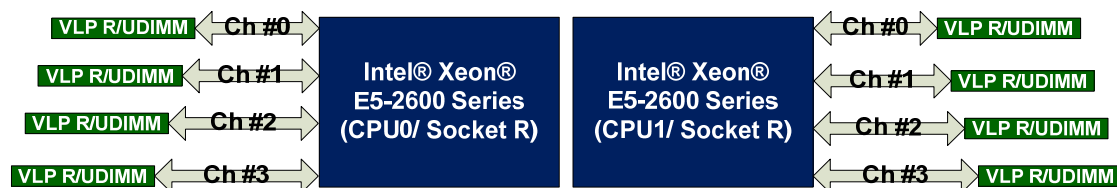


Figure 2.2 DIMM slots on the MIC-5332

DIMM Type	RDIMMs	UDIMMs	LRDIMMs
Size	2GB, 4GB, 8GB, 16GB and 32GB	2GB, 4GB and 8GB	8GB, 16GB and 32GB
Speed	1066 / 1333 / 1600		1066 / 1333
Ranks	SR, DR, QR (only for 1066/1333)	SR, DR	QR

Table 2.7: Supported DIMM Configurations



Note:

- ◆ 2G, 4G and 8GB DDR3 DRAM technologies are supported for these devices:
 - ✧ UDIMMs x8, x16
 - ✧ RDIMMs x4, x8
 - ✧ LRDIMMs x4, x8
- ◆ Up to 4 ranks supported per memory channel: 1, 2 or 4 ranks per DIMM.
- ◆ Supports a maximum of 256GB DDR3-1600 memory.

2.3.2 RAS Mode

Four DRAM RAS modes are supported by the memory controller which can be configured in BIOS setup menu.

◆ Independent Channel Mode (Default)

Channels can be populated in any order in Independent Channel Mode. All four channels may be populated in any order and have no matching requirements. All channels must run at the same interface frequency, but individual channels may run at different DIMM timings (RAS latency, CAS latency, etc.).

◆ Rank Sparing Mode

In Rank Sparing Mode, one rank is a spare of the other ranks on the same channel. The spare rank is held in reserve and is not available as system memory. The spare rank must have identical or larger memory capacity than all the other ranks (sparing source ranks) on the same channel. After sparing, the sparing source rank will be lost.

◆ **Mirrored Channel Mode**

In Mirrored Channel Mode, the memory contents are mirrored between Channel 0 and Channel 2 and also between Channel 1 and Channel 3. As a result of the mirroring, the total physical memory available to the system is half of what is populated. Mirrored Channel Mode requires that Channel 0 and Channel 2, and Channel 1 and Channel 3 must be populated identically with regards to size and organization. DIMM slot populations within a channel do not have to be identical but the same DIMM slot location across Channel 0 and Channel 2 and across Channel 1 and Channel 3 must be populated the same.

◆ **Lockstep Channel Mode**

In Lockstep Channel Mode, each memory access is a 128-bit data access that spans Channel 0 and Channel 1 and Channel 2 and Channel 3. Lockstep Channel mode is the only RAS mode that allows SDDC for x8 devices. Lockstep Channel Mode requires that Channel 0 and Channel 1, and Channel 2 and Channel 3 must be populated identically with regards to size and organization. DIMM slot populations within a channel do not have to be identical but the same DIMM slot location across Channel 0 and Channel 1 and across Channel 2 and Channel 3 must be populated identically.



Note:

- ◆ The memory channel mode can be configured in BIOS setup menu described in **Chapter 5, AMI BIOS Setup**.
- ◆ Regarding the correct installation of memory modules, please refer to Section 3.2, Memory for further details.

2.4 Ethernet Interface

2.4.1 Base Interface

The MIC-5332 uses Intel® i350-AM4 LAN controller, connected to the Intel® Xeon® E5-2600 series Processor (CPU0) through a PCIe x4 interface to provide dual GbE ports for the Base Interface.

The Intel® Ethernet Controller I350 is a single, compact, low power component that supports quad port and dual port gigabit Ethernet designs. The device offers four fully-integrated gigabit Ethernet media access control (MAC), physical layer (PHY) ports and four SGMII/SerDes ports that can be connected to an external PHY. The I350 supports PCI Express* (PCIe v2.1 (2.5GT/s and 5GT/s)).

The device enables two-port or four port 1000BASE-T implementations using integrated PHY's.

The MIC-5332 also supports PXE boot and SoL (Serial-over-LAN) over the Base Interface channels. PXE boot can be enabled “Launch PXE OpROM” through the BIOS setup menu (see **Section 5.4., Advanced BIOS Features Setup**). Information about PXE expansion ROM configuration is also provided in this section.

The Intel i350 controller supports side-band functionality. This side-band interface (NC-SI) is used by the IPMC to establish LAN sessions, to enable RMCP/RMCP+ based communication to the management part. See **Section 4.6, Serial-over-LAN** for details on setting up connections to the BMC.

2.4.2 Fabric Interface

The MIC-5332 uses an Intel® 82599 dual XAUI port 10GbE controller for Fabric Interface channels 1 and 2. In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCIe packet traffic across its transaction, link, and physical/logical layers. The Intel® 82599 makes a significant improvement on many Ethernet features such as I/O acceleration, security enhancement, and virtualization. Flow director boosts 10GbE performance & efficiency on multi-core CPUs, and VMDq2 increases the number of virtual machine up to 64. For additional technical details of Intel® JL82599EB, please visit www.intel.com.

Additional fabric channels (3 and 4) can be supported via the FMM (see Appendix DE). Redrivers for e-keying support and for improved backplane signal integrity are provided onboard the MIC-5332 for these fabric channels.

The MIC-5332 Fabric Interface supports PICMG 3.1 Options 1 or 9.

2.4.3 I/O Ethernet Interface

There are three I/O LAN ports on the MIC-5332 front panel, which are implemented using Intel® i350-AM4 quad port GbE controller and 82579 gigabit Ethernet PHY (MAC provided by C604 PCH). The MIC-5332 can support either two SFP or two RJ45 connectors for the i350-AM4 front ports as build option..

The PCH MAC and the 82579 PHY additionally support one RJ45 port at the front panel.

Interface	Connection	Chip	Media	Speed	PXE/SoL
Base Interface	Backplane	Intel® i350-AM4 Ports 0, 1	Copper	10/100/1000 Mb/s	✓
Fabric Interface	Backplane	Intel® 82599	BX4 or XAUI	1/10 Gb/s	

I/O Interface	Front Panel	Intel® i350-AM4 Ports 2, 3	Copper or Fiber	10/100/1000 Mb/s	✓
		Intel® 82579	Copper	10/100/1000 Mb/s	

Table 2.8: Ethernet Interface Link Speed Configuration

2.5 Zone 3 Interface (RTM)

The MIC-5332 supports the following connectivity to an optional RTM through the zone 3 interface (please refer to the [Appendix D](#), Zone3 interface (RTM) pin-out):

- ◆ 1x PCI Express x16
- ◆ 1x PCI Express x4
- ◆ 4x USB 2.0
- ◆ 2x UART
- ◆ 4x SAS 3Gbps and 2x SATA 3Gbps

The rear transition module (RTM) is generally used to provide the additional I/O extension for the main board. It is managed with an on-board MMC and is fully hot swappable. Customer may ask for a customized RTM (please contact your Advantech representative) or choose the Advantech RTM-5104. For detailed specifications, please refer to table 2.9. For the detailed pin list of the Zone 3 interface, please see **Appendix D, Zone 3 Interface (RTM) Pin Assignment**.

Model Name	Storage	USB	LAN	COM	FMM Support	External SAS Connectors
RTM-5104SE	2x SAS	1	2x RJ45	1x miniUSB	✓	
RTM-5104ME	4x MO-297	1	2x RJ45	1x miniUSB	✓	
RTM-5104NE	2x SAS	1	2x SFP	1x miniUSB & 1x RJ45		2x miniSAS

Table 2.9: Advantech RTM-5104 Specifications



Note:

- ◆ Please contact with your local Advantech sales to get the more information about RTM-5104.

2.6 Fabric Mezzanine Module (FMM)

The MIC-5332 supports the following connectivity to an optional FMM board connected via an on board connector (FMM1), or on an external RTM board.

The FMM board is generally used to provide an option to expand the feature sets, both for the main board and RTM board. It is managed by the main board's IPMC or RTM board's MMC, but does not support the hot-swap function. Customers may request a customized FMM (please contact your Advantech representative) or choose from the following Advantech FMM-5000 options. For detailed specifications, please refer to table 2.10.).

Model Name	Description	Chip	I/O
FMM-5001B	Additional 10GbE Support for Dual-Dual Star FI	Intel® 82599	N/A
FMM-5001F	Additional 10GbE Support for Dual-Dual Star FI	Intel® 82599	2x SFP+
FMM-5002	Server Graphic Support for Debug/Bring Up	SM750	1x VGA port

Table 2.10: Advantech FMM-5000 Series Specifications

Chapter 3

Installation

This chapter describes the procedure to install the MIC-5332 into a chassis. Peripherals (DIMMs, SSD) installation, jumper setting and LED definition are also described here.

3.1 Processor

The MIC-5332 is shipped with two CPUs and heat sinks installed. Please do not attempt to remove the heat sinks, or the cooling performance will be affected. Tampering with the heat sinks will result in loss of warranty.



3.2 Memory

3.2.1 Requirement

As described in Section 2.3, DDR3 DIMMs, the MIC-5332 supports 8 x DDR3 VLP (very low-profile, 0.72inch; 18.29mm) un-buffered/registered ECC SDRAM DIMMs. To allow proper MIC-5332 functionality, please comply with population requirements when installing memory modules:

- ◆ Mixing of Registered and Unbuffered DIMMs is not allowed.
- ◆ To optimize the memory performance by balanced sharing the load on each channel of a socket, Advantech **requires** to use the identical memory modules, with the same density, rank, speed, timing parameters, and other factors.
- ◆ Although unbalanced configurations might work, they are not supported by Advantech.
- ◆ For supported memory characteristics, please refer to Table 2.7, Supported DIMM Configurations.



3.2.2 Memory Installation

Please review the following procedures for memory installation:

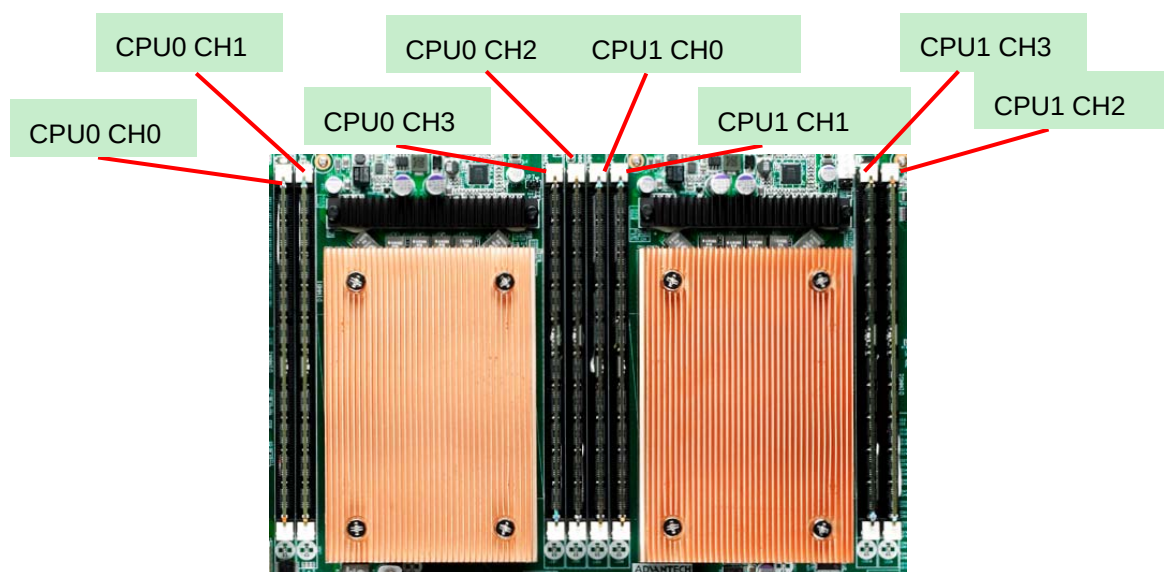


Figure 3.1 MIC-5332 DIMM Slots Overview

1. Open the ejector on the empty DIMM socket where you want to install the DIMM.
2. Insert the memory module into the empty slot. Please align the notches on the module with the socket keys.
3. Push the module into socket until the ejectors firmly lock.
4. Repeat steps 1~3 for the remaining modules to be populated.
5. Install the MIC-5332 into the chassis and boot the board, checking if all the memory information shown in BIOS menu is correct. (See Section 3.3, Console Terminal Setup and Section 3.4, Installing the MIC-5332)

To remove DIMM modules, please follow the instructions listed below:

1. Remove the MIC-5332 from the chassis. (See Section 3.4, Installing the MIC-5332)
2. Choose one DIMM to remove and push the DIMM ejector on each side of the DIMM socket outward simultaneously. The module shall pop out by itself.
3. Close the ejectors of the empty DIMM socket.
4. Repeat steps 2, 3 for the remaining modules to be removed.

3.3 Console Terminal Setup

The MIC-5332 contains five serial interfaces (listed as below). More details about setup will be described through an example, to show how to setup the console for the MIC-5332 with the following example sections.

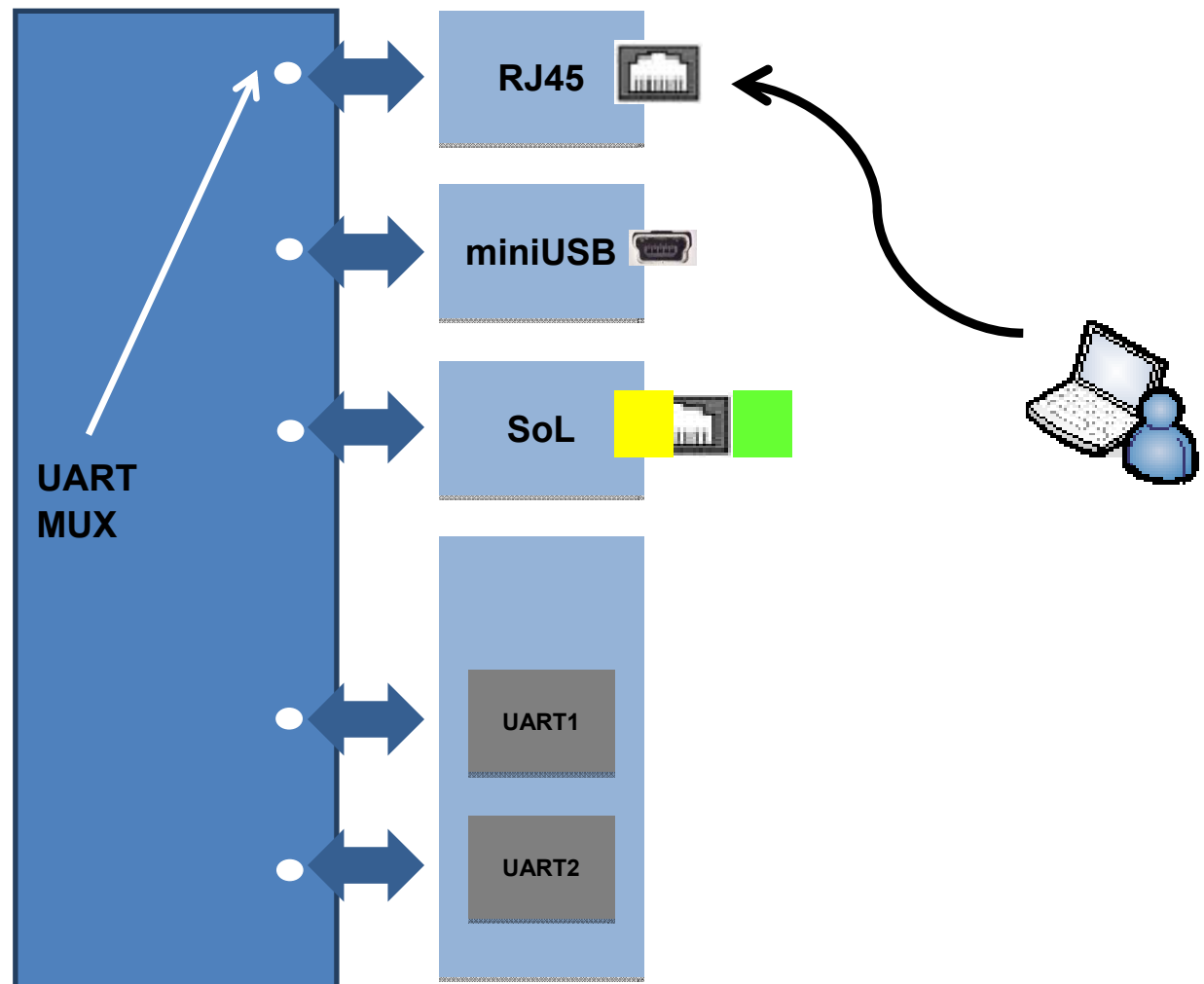
- ◆ COM1 (RJ45) on the front panel
- ◆ COM2 (miniUSB) on the front panel
- ◆ Serial-over-LAN, SoL (via I/O or BI Ethernet interface)
- ◆ UART1 routed to Zone 3
- ◆ UART2 routed to Zone 3

3.3.1 UART Multiplexer

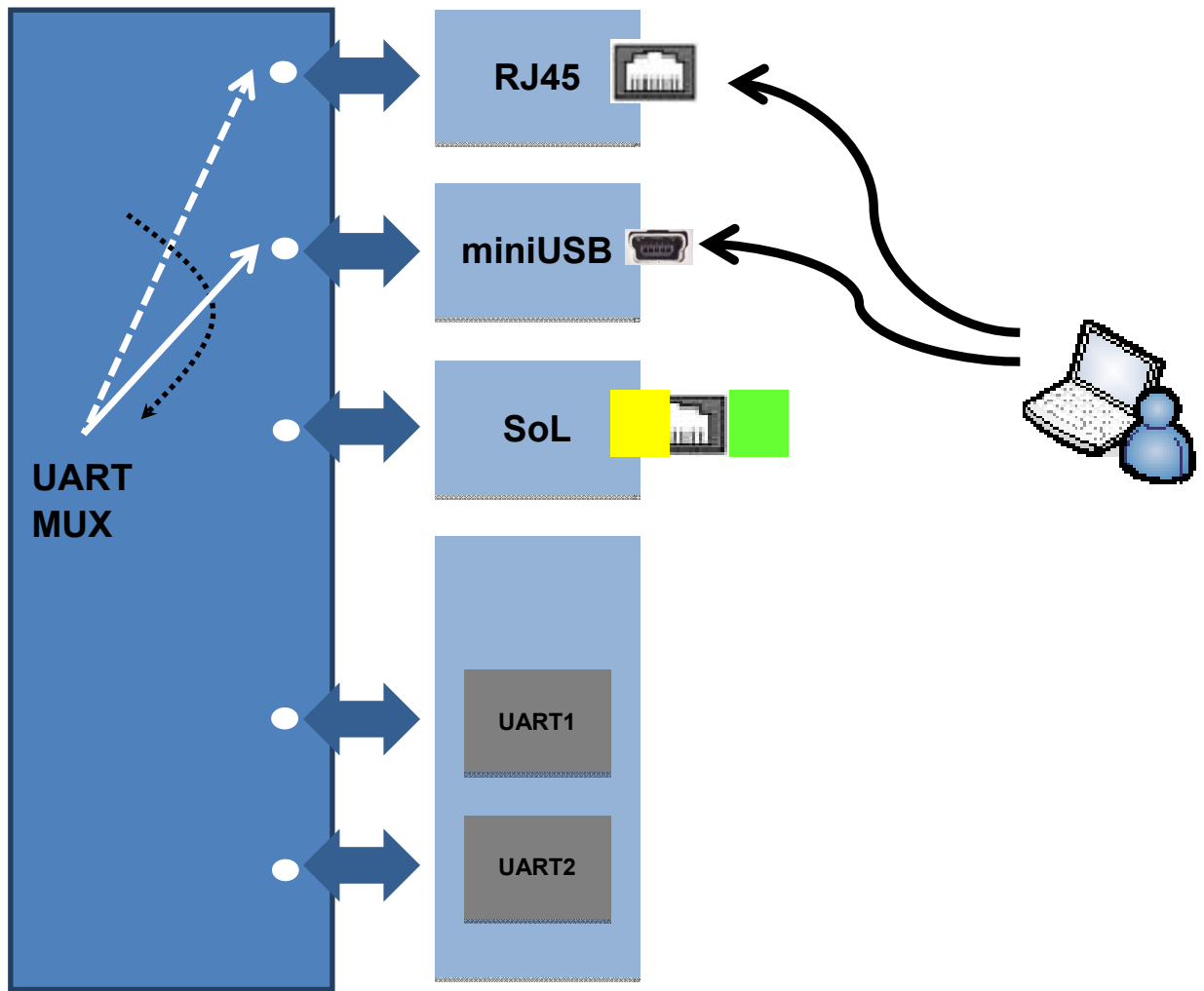
The UART multiplexer can be set to route the console to any of the connections mentioned above. By default the UART multiplexer is set to automatic mode, that means, the mux will automatically switch to the connection except the SOL, where an input character is received.

For example, when a RJ45 to DB9 cable is plugged into the MIC-5332, by detecting a character entered through the cable, the UART multiplexer will automatically bridge the console to the terminal PC through this interface. Once another mini-USB cable is

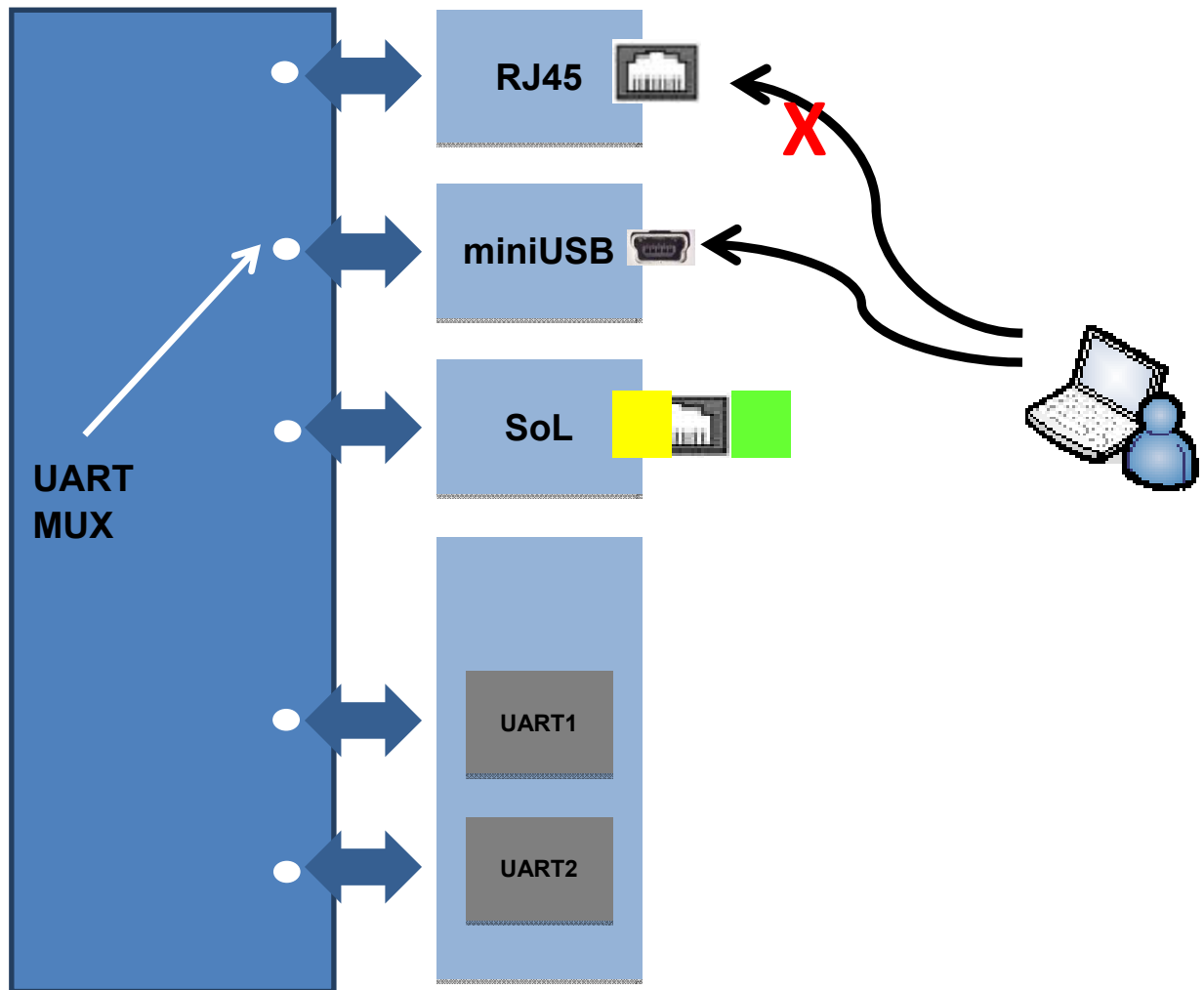
connected and the user enters any character, the multiplexer will then switch the output to this interface as this is the latest request. The previous RJ45 link will consequently become disconnected.



Step1. User establishes the console link through any available output (e.g. RJ-45)



Step2. When the user plugs another console cable into the MIC-5332, (e.g. miniUSB), the UART MUX will switch the output from RJ45 to this new interface (last in, first serve rule)



Step3. The original link (RJ-45) becomes disconnected

Figure 3.2 UART Multiplexer Switching Mechanism

RJ45 (COM1)

For a terminal PC to connect to the console function on the MIC-5322 with a RJ45 to DB9 cable, no additional driver is needed.

Prerequisite:

- ◆ *RJ45 to DB9 cable*

mini-USB (COM2)

The MIC-5332 uses a USB-to-UART bridge called CP2102-GM from Silicon Labs® to

convert data traffic between USB and UART formats. This chip includes a complete USB 2.0 full-speed function controller, bridge control logic, and a UART interface with transmit/receive buffers and modem handshake signals.

For a terminal PC to connect to the console function on the MIC-5332 with a mini-USB to USB cable, the CP2102 driver is available for download from Silicon Labs® website (hyperlink below), and must be installed on the terminal PC. The PC can, for example, run a Linux 2.4 or 2.6 kernel or Windows XP).

The miniUSB port is bus powered (i.e. powered by the terminal PC) and the COM port will not be lost when power cycling the blade or ATCA system.

Prerequisite:

- ◆ **Commercial mini-USB to USB cable**
- ◆ **CP2102 driver (needed to be installed on the terminal PC before using the console),**
please **download** **from**
<https://www.silabs.com/products/interface/usbtouart/Pages/default.aspx>

Serial-over-LAN, SoL

User may also establish the console via SoL function, which is described in **section 4.6, Serial-over-LAN (SoL)**.

Prerequisite:

- ◆ **RJ45 Ethernet cable and IPMITool (see section 4.6.2.1 IPMITool)**



Note:

- ◆ When SoL is used as the console terminal, please skip Section 3.3.2 and 3.3.3.

UART1 & UART2 (Zone3)

The MIC-5332 connects two UART interfaces to the Zone 3. To establish the console link through the RTM, please refer to the RTM user manual.

3.3.2 Terminal Emulator

A terminal emulator application must be available on the terminal PC in order to access the console screen. If your terminal PC runs on Microsoft Windows, a common application that can act as a client for the SSH, Telnet, rlogin, and raw TCP protocols called PuTTY can be installed and used. PuTTY was originally written for Microsoft Windows; however, it has also been ported to various Unix-like operating systems. It is available as open source software for download from the internet.

3.3.3 PuTTY Configuration

Assuming both the CP2102 driver and PuTTY have been installed successfully on the terminal PC with Microsoft Windows, the user can check the COM port (UART) number under “COM and LPT” in the “Device Manager”, which can be accessed by entering the “Control Panel” followed by opening up “System” and then “Hardware”. Let us assume the CP210x USB to UART Bridge Controller has been assigned with “**COM12**”, you can open up PuTTY and begin the configuration as shown below. If you use the RJ45 (COM1) and a serial port on the terminal PC, please use the COM port number of that serial port instead of “COM12”.

- ◆ Specify **COM12** under serial line and **115200** for speed, no parity, no flow control.
- ◆ Check **Serial** for connection type.
- ◆ Click the “Open” button and a PuTTY terminal screen will appear.

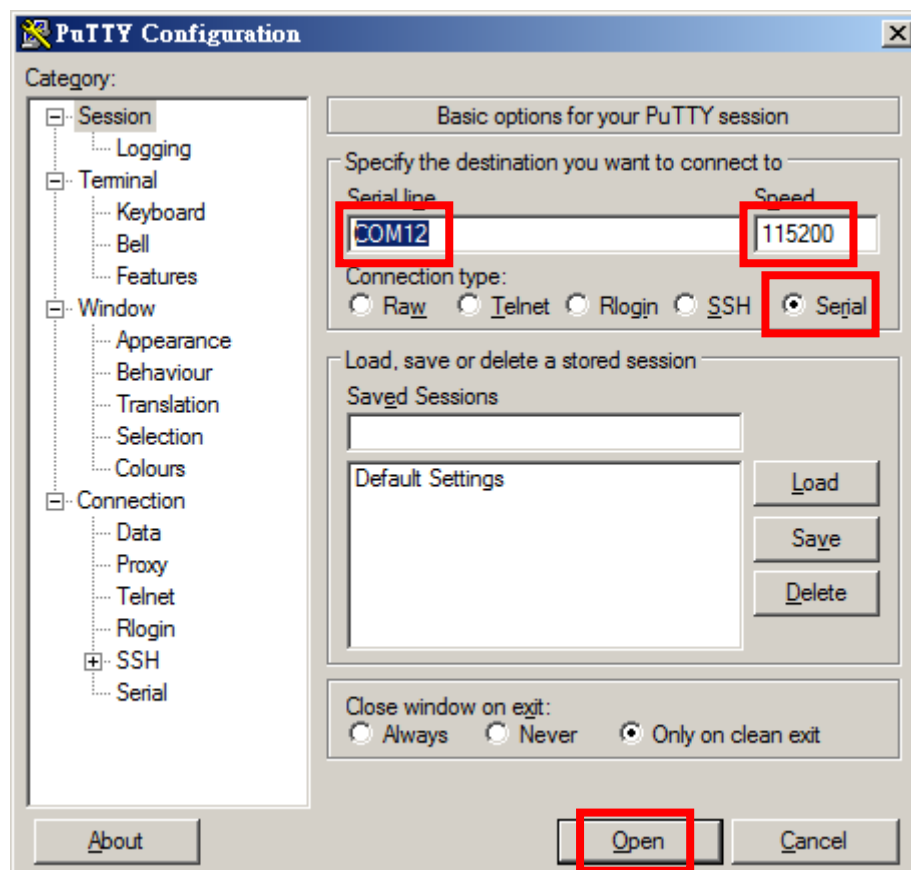


Figure 3.3a PuTTY Configuration

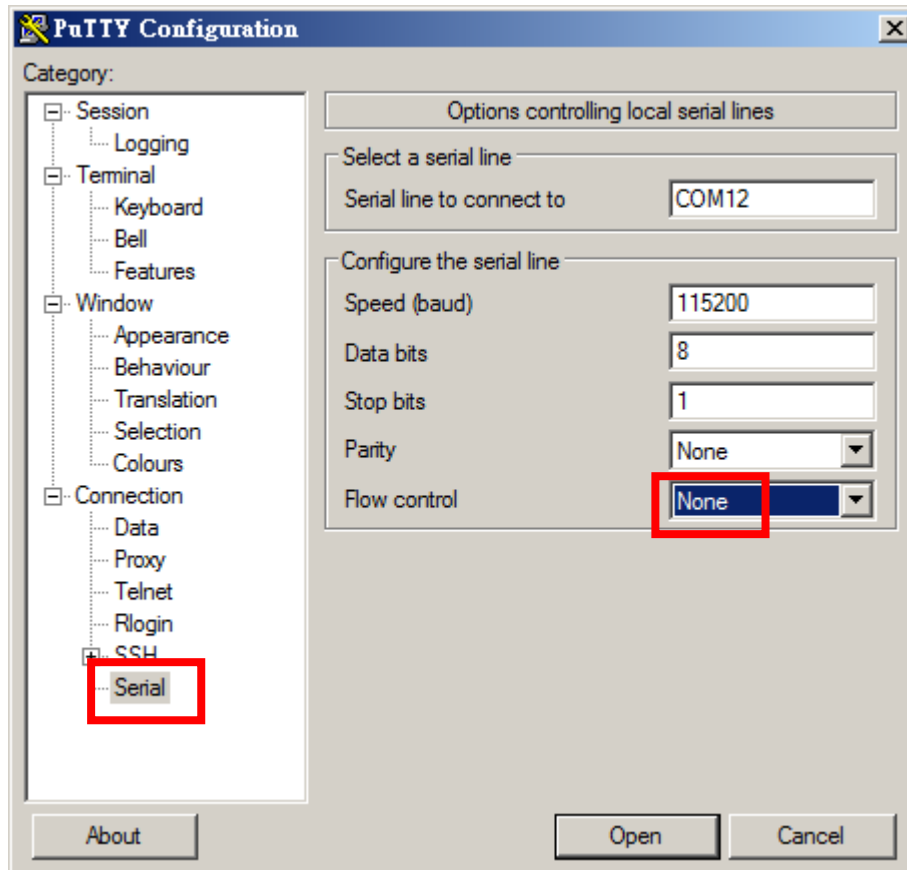


Figure 3.3b PuTTY Configurations

If the connection is successful and the user enters BIOS setup menu, upon boot the MIC-5332 BIOS setup menu will be displayed on the PuTTY screen.

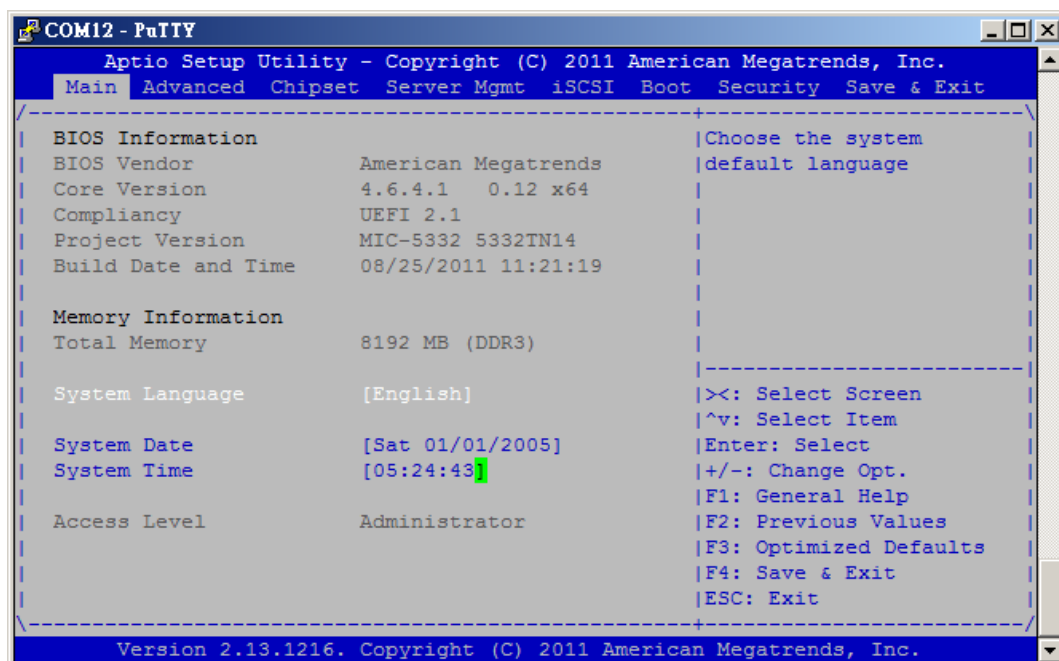


Figure 3.4 MIC-5332 BIOS setup menu shown on PuTTY screen

3.4 Installing the MIC-5332

3.4.1 MIC-5332

To install MIC-5332 into the chassis:

1. Leave the ejector handles in the open position.
2. Choose a node slot in chassis, and align the PCB edge to the card guide rail.*
3. Carefully slide the MIC-5332 into the system until the connector contacts start to mate into the backplane. Make sure the front panel alignment pin falls into the receptacle.

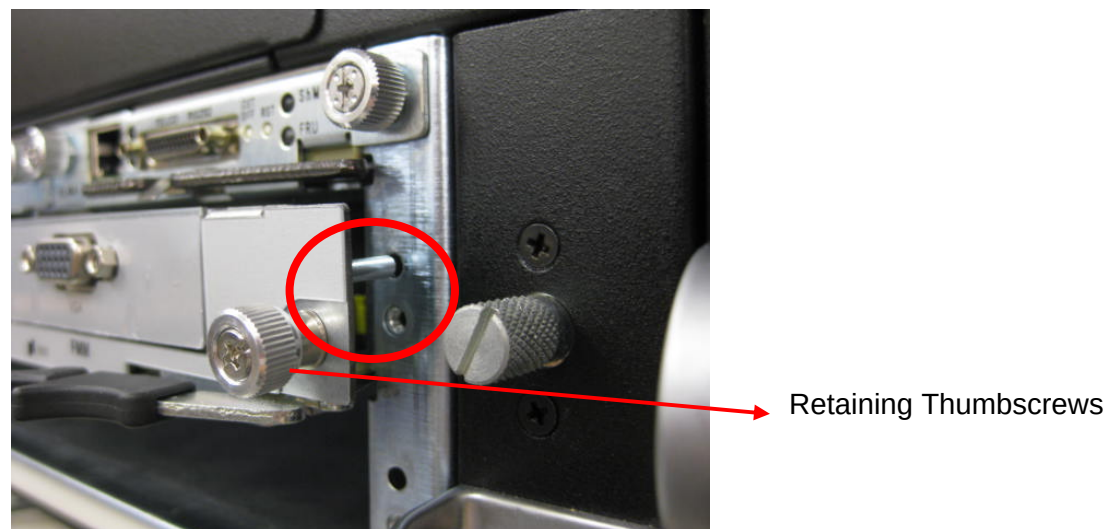


Figure 3.5 Alignment pin slides into the receptacle

4. Hold both handle ejectors on either side of the board, and then close them to make the board becomes fully seated. Make ensure the handles are latched securely.
5. Fasten the retaining thumbscrews.
6. The blue hot-swap LED on the front panel will show a “ON→Blink→OFF” transition to indicate a normal power-on sequence of the MIC-5332. Once the FW and payload has been successfully activated, the PICMG 3.0 LEDs will be shown as below:

Out of Service	Health	Hot swap

Table 3.1 PICMG3.0 LEDs Definition

All the LEDs status shown on the front panel is listed in Section 3.6, Jumper Setting & LED Definition.



Note:

- ◆ Regarding the slot information, please refer to the backplane/chassis manual
- ◆ The MIC-5332 also supports hot-swap, i.e. no need to turn off the chassis power before installing the board.

To extract the MIC-5332 from the chassis:

1. Unlock the ejector handle at the bottom side, next to the FMM bay.
2. The extraction request will be delivered to the IPMC. The IPMC will perform a graceful shutdown of the ACPI aware operating system. The blue hot-swap LED will start blinking once the ejector handle is unlocked.
3. After the x86 subsystem on the blade has been powered down, the blue hot-swap LED will light up, which indicates the board is ready to be removed.
4. Unfasten the retaining thumbscrews.
5. Unlock the other handle, and fully open both handles (push handles outwards) to extract the board.
6. Pull the MIC-5332 out of the chassis.



Figure 3.6 Unlock the ejector handle



Caution!

- ◆ DO NOT attempt to extract the board when blue LED is off or blinking. This may cause non-recoverable damage to the board.

3.4.2 FMM (Option)

The MIC-5332 supports one FMM slot for feature expansion, such as VGA output, additional 10GbE support for dual-dual star FI, and Intel® QuickAssist support (for details, please refer to table 2.10). It is assumed that MIC-5332 is shipped with the

FMM installed. Mounting instructions are still provided here to support customer development as well as inhouse RMA and repair.

For installation of the FMM, please follow the below procedures:

1. Locate the FMM site on the blade (refer to figure 3.9) and make sure the module and the carrier connectors are aligned. Insert the FMM module until the connector is firmly seated in the socket.
2. Install the screws (refer to figure 3.10), and power on the MIC-5332 to make sure the installation is completed.
3. To remove the FMM, follow the procedure in reverse.

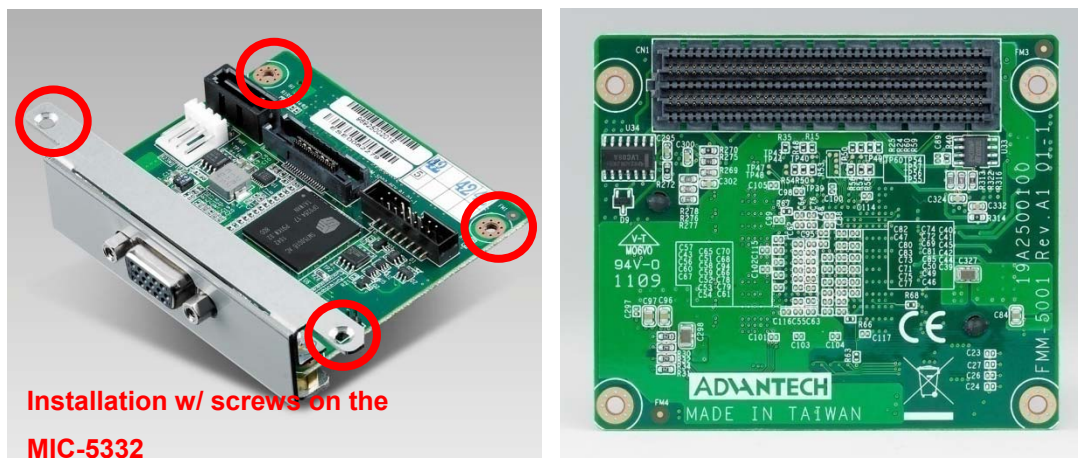


Figure 3.7 FMM Module top (left) and bottom (right) views

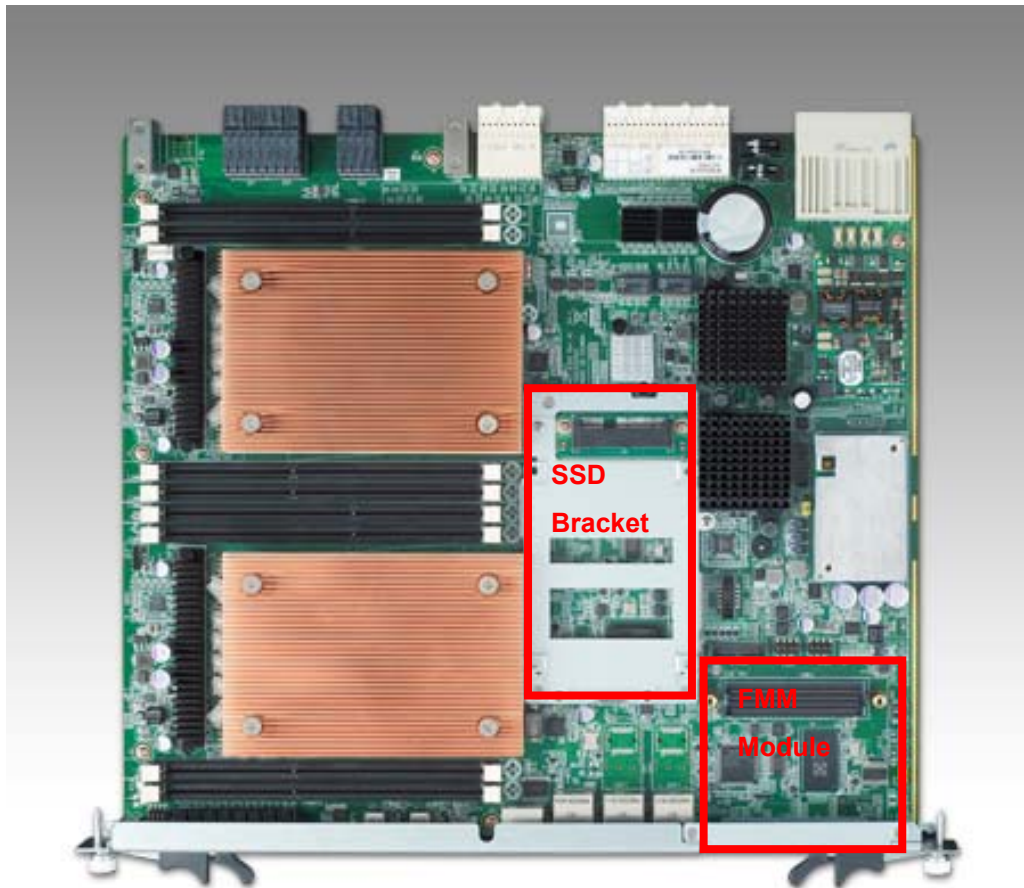


Figure 3.8 MIC-5332 w/ FMM module and SSD Bracket locations

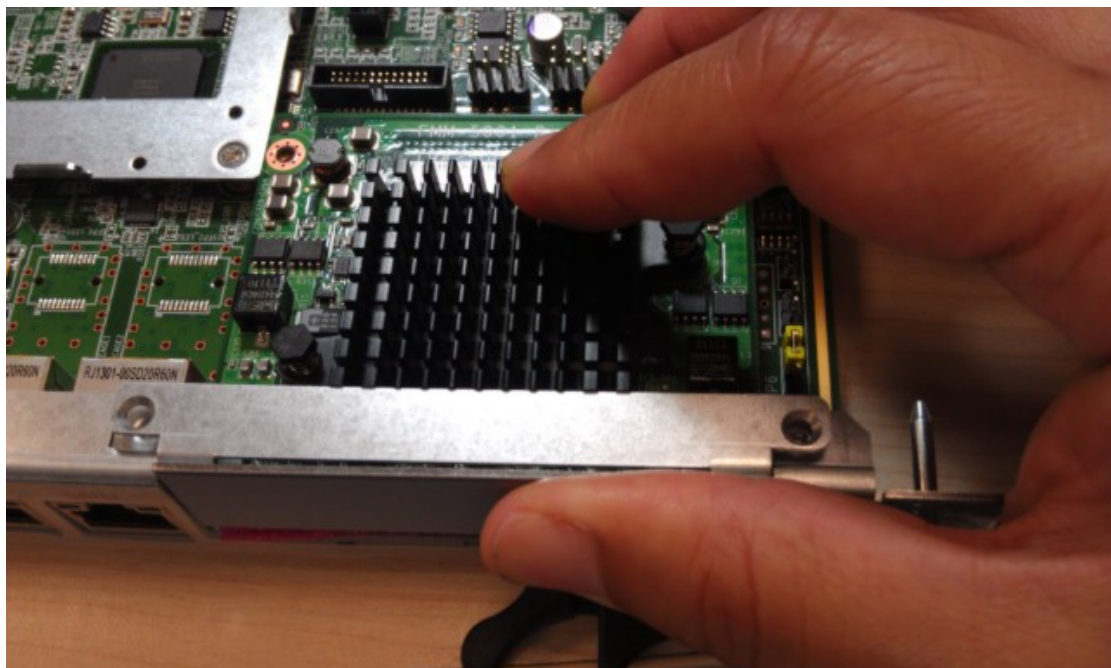


Figure 3.9 Locate the FMM site on the blade

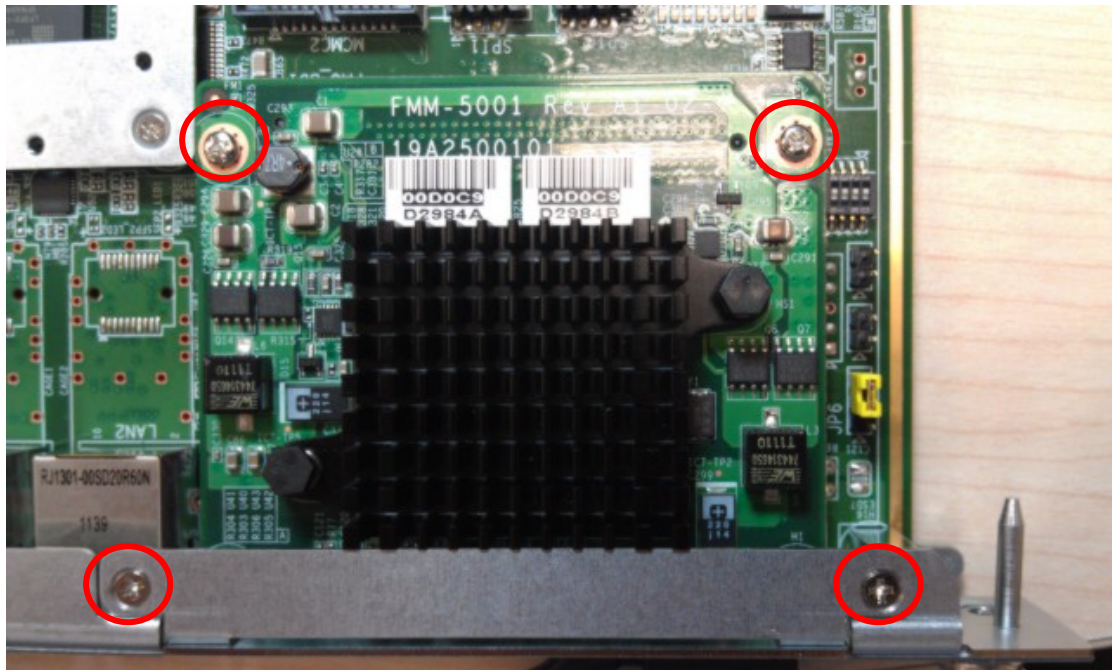


Figure 3.10 Install the screws

3.4.3 RTM (Optional)

For installation of the RTM, please refer to the RTM user manual. Please make sure that the RTM used in conjunction with the MIC-5332 is compliant. Please contact your Advantech representative to obtain a list of compliant RTMs (the current compliant RTM at the time of publication is the RTM-5104).

3.4.4 Storage (Optional)

Solid State Drive (SSD) or CFast cards are available to be installed on the MIC-5332. The MIC-5332 can support one 2.5" SSD, or two CFast cards. It is an option by customer request, and the MIC-5332 will need to be installed with a specific daughter board and bracket from the factory. For more details, please contact your Advantech representative to obtain a list of compliant SSDs and CFast cards.

3.4.5 Front Panel

The MIC-5332 is 100% compatible to AdvancedTCA specifications. All LED signals are shown on the front panel. Users can refer to section 3.6, "LED definition" to know the details of the board operating status.

- ◆ Please note that LAN1 and LAN2 are optional devices. They can be populated from the factory with SFP connectors to support fiber cables and related devices, or a regular RJ45 connector for common devices which support Cat 5/5e.
- ◆ Button1 and 2 are reserved for customized. Button1 is set as a reset function by default, while Button2 is not assigned. Users can define the functions for each.

For details, please contact your Advantech representative to obtain further support.

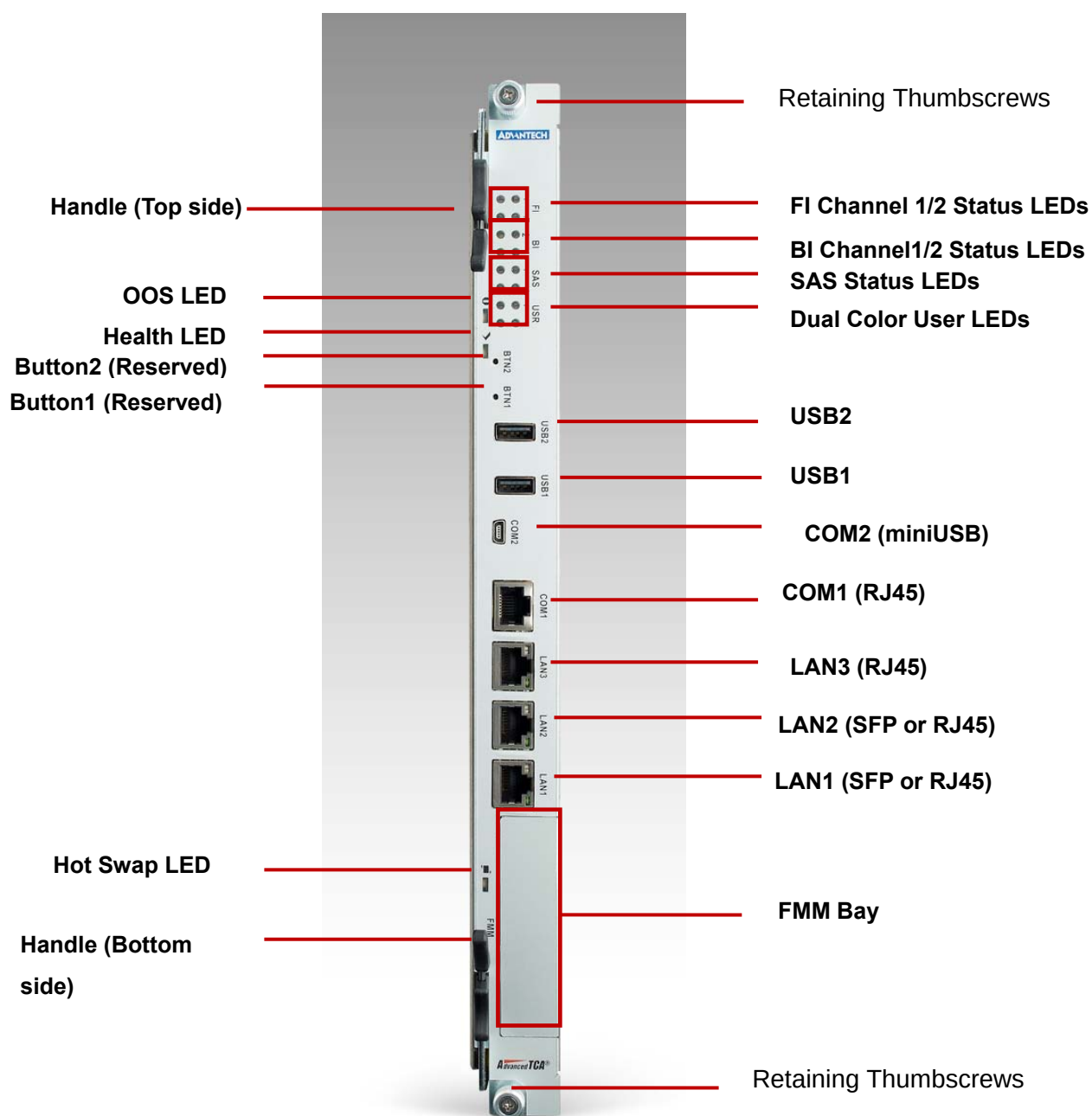


Figure 3.9 MIC-5332 Front Panel Configuration

3.4.6 LED Definition

This section describes how to identify the system operating status via LED signals from the front panel. Before starting, please refer to table 3.2 to learn the LED signal identification in this manual. In the following section, we take amber as an example:

Display	Status
	Bright
  ... 	Blink
	Off

Table 3.2 LED Signal Identification

LED Name		Function	Display
FI port	1/2/3/4	Speed/Link/ Active	10Gb/s Link ... 10Gb/s Active 1Gb/s Link ... 1G Active No Link
BI Port 1/2	S	BI port 1/2 Speed	1Gb/s 100Mb/s 10Mb/s
	L	BI port 1/2 Link / Active	Link ... Active No Link
SAS Status	1/2/3/4	Active/Failure	Active Failure
USR Status	1/2/3/4	N/A	User defined User defined
LAN Port	1/2/3	Speed	1Gb/s 100Mb/s 10Mb/s
		Link/Active	Link ... Active No Link
		Out of Service	System out of service System normal
		Health Status	FW active, payload enabled ... FW active, payload disabled FW is not active
		Hot swap	Board is not activated (ready to be swapped) ... Board is de-/activating, unsafe to swap Board is active, unsafe to swap

Table 3.3 LED Definition

**Note:**

FI channel 3 and 4 support is optional and only active when populating with the FMM-5001BE on the FMM site of the MIC-5332.

3.4.7 Jumper Settings

This section describes the jumpers on the MIC-5332 for reference. In normal operation, users are not to access or modify jumpers.

Jumper	Feature	Setting		Operation
JP1	Clean CMOS	1-2 Closed		Normal Mode (Default)
		2-3 Closed		Clean CMOS
JP6	GND Connection	2-3 Closed		Shelf GND open to logic GND, (Default)
		1-2 Closed		Shelf GND short to logic GND

Table 3.4 Jumper Settings

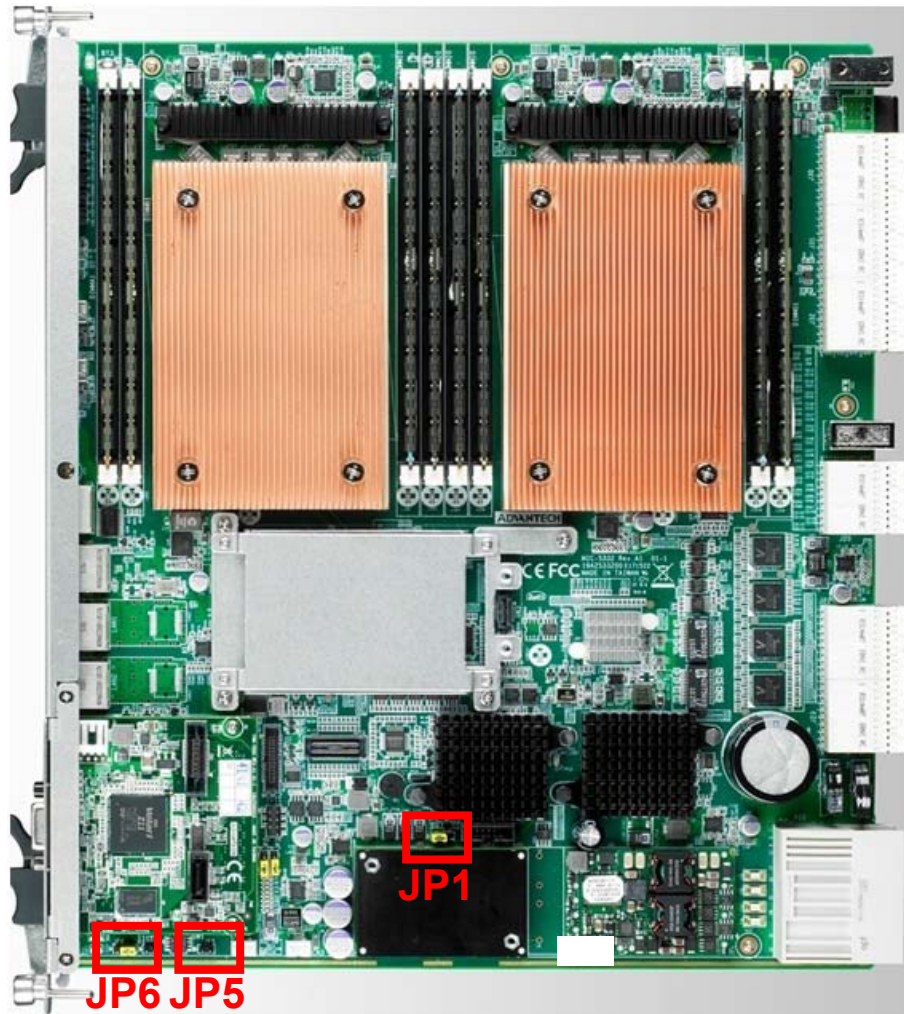


Figure 3.10 Jumper Locations

Chapter 4

Hardware Management

This chapter describes the IPMC firmware features.

4.1 Overview

A complete management mechanism is strength of AdvancedTCA. An on board IPMC (Intelligent Platform Management Controller) is in charge of collecting board information (e.g. sensor events, health status, hot swap, etc.), log events to a repository, and forwards them to the ShMC (Shelf Manager Controller). The shelf manager will take actions based on these messages as needed.

4.2 Intelligent Platform Management Controller

A NXP LPC1768 microprocessor and a Lattice LatticeXP2 FPGA form the management block of the MIC-5332. The system management solution is based on Advantech IPMI Core G02 which is Advantech's ATCA System Management implementation. Its core is a NXP LPC1768 Cortex-M based CPU running on an RTOS. For the list of supported IPMI commands by Advantech, please refer to **Appendix A, IPMI/PICMG Command Subset Supported by IPMC**.

A Lattice LFXP2F17 FPGA is used to provide additional connectivity for the IPMC and payload. It provides extension interfaces with configurable routing options as well as some additional stand-alone functionality.

One of the very basic benefits of Advantech IPMI Core G02 is the high level of flexibility. Its modular structure allows the same firmware core to be [used on different xTCA platforms, sharing](#) a high percentage of identical code.

4.2.1 IPMC Interface

In this section, we will describe the four different IPMC communication interfaces (listed as below) of the MIC-5332.

- ◆ ***IPMC ↔ ShMC: IPMB-0***
- ◆ ***IPMC ↔ RTM: IPMB-L***
- ◆ ***IPMC ↔ payload: KCS***
- ◆ ***IPMC ↔ Ethernet through NC-SI on BI/IO***

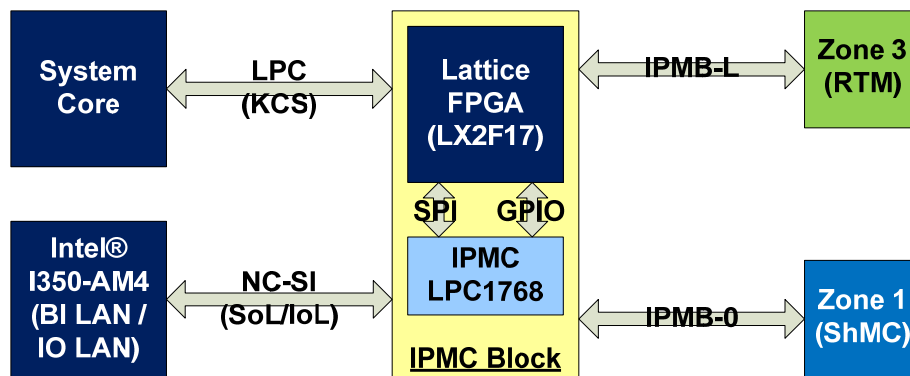


Figure 4.1 IPMC Interface Block Diagram

4.2.1.1 IPMB-0 Interface

The IPMB0 interface is the communication path between the ShMC and IPMC through Zone 1. Two-way redundant IPMB-0 channels (IPMB0-A and IPMB0-B) provide immunity against failures of one of IPMB-0 channels.

For a request received over IPMB0-A, the response will be sent over IPMB0-B. Any requests that time out are retried on the redundant IPMB bus. The IPMC monitors the bus for any link failure and isolates itself from the bus if an error is detected.

The IPMB address of IPMC is determined by Hardware Address pins (HA[7:0]) on the Zone 1 connector. The manual of the chassis/backplane contains information that allows relating the physical IPMB address to the slot location within the chassis.

4.2.1.2 IPMB-L Interface

IPMB-L is the interface between the IPMC and a Module Management Controller (MMC) on a compliant RTM such as the RTM-5104. It is connected to the IPMB-L bus through I²C bus isolators.

4.2.1.3 System Interface

The x86 subsystem (referred to as payload) may communicate with the IPMC via a KCS interface. The KCS commands will be transferred through a Low Pin Count (LPC) interface between the Patsburg-B PCH and the IPMC.

4.2.1.4 LAN (NC-SI) Interface

The Intel i350-AM4 controller provides a sideband interface (NC-SI) that can be used by the IPMC. Serial-over-LAN (SoL) uses the RMCP+ protocol over this interface to encapsulate serial data in network packets and pass them between the payload and the remote console. IPMI over LAN (IoL) may be used to communicate with the IPMC over the BI or IO Ethernet LAN ports connected to the i350-AM4.

Note:

The IPMC firmware provides an OEM IPMI command to allow users to switch the IMPC/FPGA connected NC-SI interface between the front panel LAN IO and the Base interface LAN controllers and also to select between the 2 IO and BI connections. See below the description of the corresponding OEM commands:

LAN controller interface selection

The BMC firmware provides an OEM IPMI command to allow users to switch the BMC connected NC-SI interface between two front panel LAN IO RJ-45 connector and the Base interface (0/1). These commands can be used to read out the actual selected IPMI-over-LAN / Serial-over-LAN interface and to change the selection.

LAN controller interface selection settings:

00h: Front panel LAN IO

01h: LAN BI (default)

Read LAN Interface selection:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x00
```

Response:

```
39 28 00 <setting>
```

Change LAN Interface selection:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x00 <setting>
```

Response:

```
39 28 00
```

LAN controller channel selection and priority

In addition to the selected LAN controller interface, users may need to configure each single LAN controller channel (port) as dedicated NC-SI interface to the BMC. Additional OEM commands for the configuration of the NC-SI LAN controller channel selection and priority are provided to allow a flexible configuration.

LAN channel selection priority setting list:

0 = The first channel that links up, gets the NC-SI connection to the BMC.

1 = Channel 1 is the preferred port if it is up, otherwise use channel 2 if it is up.

2 = Channel 2 is the preferred port if it is up, otherwise use channel 1 if it is up.

3 = Channel 1 is the only allowed port, always use it, never change to channel 2.

4 = Channel 2 is the only allowed port, always use it, never change to channel 1.

The NC-SI LAN controller channel setting will be stored permanently (non-volatile EEPROM). The default value is 0.

Read LAN channel selection priority:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x01
```

Response:

```
39 28 00 <setting>
```

Change LAN channel selection priority:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x01 <setting>
```

Response:

```
39 28 00
```

4.2.2 System Event Log (SEL)

The IPMC supports a non volatile System Event Log (SEL), which stores events of onboard sensors as well as hosted FRUs such as the RTM modules. The SEL contains 8192 bytes (512 sel entries), and new events will overwrite the old ones after the SEL is full. Besides putting logs in local EEPROM, these events will also be delivered to Shelf Manager via IPMB-0 interface.

4.3 Board Information

The board information is stored in the FRU EEPROM. User may get the information via IPMI command: *fru*.

Field description	Board information
Format version	0x01
Board area length	(calculated)
Language code	0x19(English)
Manufacturer date/time	(Based on manufacturing date)
Board manufacturer type/length	0xC9
Board manufacturer	Advantech
Board product name type/length	0xC8
Board product name	MIC-5332
Board serial number type/length	0xCA
Board serial number	(10 characters, written during manufacturing)
Board part number type/length	0xC8
Board part number	MIC-5332
FRU file ID type/length	0xCC
FRU file ID	frudata.xml
Additional custom Mfg. Info fields.	(unused)
C1h (No more info fields)	0xC1
00h (unused space)	0x00 0x00 0x00 0x00
Board area checksum	(calculated)

Table 4.1 Board Information Area

Field description	Board information
Format version	0x01
Product area length	(calculated)
Language code	0x19(English)
Product Manufacturer type/length	0xC9
Product manufacturer	Advantech
Product name type/length	0xC8
Product name	MIC-5332
Product part/model number type/length	0xC8
Product part/model number	MIC-5332
Product version type/length	0xC5
Product version	A1 03
Product serial number type/length	0xCA
Product serial number	(10 characters, written during manufacturing)

Assert Tag type/length	0xC0
Assert Tag	(unused)
FRU File ID type/length	0xCC
FRU File ID	frudata.xml
Custom product info area fields	(unused)
C1h (no more info fields)	0xC1
00h (any remaining unused space)	(unused)
Product area checksum	(calculated)

Table 4.2 Product Information Area

4.3 Sensors

The IPMC Firmware supports the following hardware sensors monitoring: onboard voltage sensors, onboard analog/discrete temperature sensors and power input module sensors. According to the IPMI specification, sensor event thresholds are classified as Non-critical, Critical, or Non-recoverable. When different thresholds are reached, different actions will be given by the shelf manager accordingly (for details, please refer to table 4.3).

Threshold	Description
UNR	Upper Non-recoverable
UC	Upper Critical
UNC	Upper Non-critical
LNC	Lower Non-critical
LC	Lower Critical
LNR	Lower Non-recoverable

Table 4.3 Sensor Threshold Description

Moreover, the IPMC Management Subsystem also registers the below logical sensors:

- ◆ PICMG Hot Swap sensors
- ◆ PICMG IPMB sensor
- ◆ BMC Watchdog
- ◆ Version change
- ◆ OEM Sensor: Integrity Sensor

Here under please find the complete list of all contained sensor data records contained in the IPMC sensor repository MIC-5332:

Sensor Name	Description
FRU Device Locator	IPMI FRU Device Locator
HOTSWAP	PICMG Frontboard Hotswap sensor
HS_RTM	PICMG RTM Hotswap sensor
BMC_WATCHDOG	IPMI Watchdog 2 sensor
FW_PROGRESS	IPMI FW Progress sensor
VERSION_CHANGE	IPMI Version Change sensor
IPMB_0	PICMG IPMB-0 status sensor
VR_HOT	Discrete sensor Voltage regulator Status
PROC_HOT	Discrete sensor Processor HOT status
THERM_TRIP	Discrete sensor CPU 0/1 Thermal Trip
BOARD_POWER	Board Power sensor
V48-CUR	Threshold sensor DC/DC converter current
HU-CAP-VOL	Threshold sensor DC/DC capacitor voltage
V48_A-VOL	Threshold sensor DC/DC input voltage
V48_B-VOL	Threshold sensor DC/DC input voltage
BAT_3_0-VOL	Threshold sensor Battery Voltage
SB_3_3-VOL	Threshold sensor AUX voltage 3.3V
SB_5_0_VOL	Threshold sensor AUX voltage 5V
PAY_3_3-VOL	Threshold sensor payload voltage 3.3V
PAY_5_0-VOL	Threshold sensor payload voltage 5V
PAY_12-VOL	Threshold sensor payload voltage 12V
LAN_1_0-VOL	LAN chip voltage i350
LAN_1_2-VOL	LAN chip voltage
LAN_1_8-VOL	LAN chip voltage i350
PCH_1_1-VOL	PCH supply voltage
PCH_1_5-VOL	PCH supply voltage
CPU0_0_85-VOL	Threshold sensor CPU-0 0.85V
CPU0_1_05-VOL	Threshold sensor CPU-0 1.05V
CPU0_CORE-VOL	Threshold sensor CPU-0 Core Voltage
CPU0_1_80-VOL	Threshold sensor CPU-0 1.80V
CPU1_0_85-VOL	Threshold sensor CPU-1 0.85V
CPU1_1_05-VOL	Threshold sensor CPU-1 1.05V

CPU1_CORE-VOL	Threshold sensor CPU-1 Core Voltage
CPU1_1_80-VOL	Threshold sensor CPU-1 1.80V
DDR_AB-VOL	Threshold sensor DDR Voltage 1.5V
DDR_CD-VOL	Threshold sensor DDR Voltage 1.5V
DDR_EF-VOL	Threshold sensor DDR Voltage 1.5V
DDR_GH-VOL	Threshold sensor DDR Voltage 1.5V
V48-TMP	Threshold sensor DC/DC converter temperature
INTAKE0-TMP	Threshold sensor LM75 intake temperature
POWER-TMP	Threshold sensor LM75 near PIM
OUTLET1-TMP	Threshold sensor LM75 exhaust temperature
PCH-TMP	Threshold sensor PCH temperature
CPU_0-TMP	Threshold sensor CPU-0 temperature (PECI)
CPU_1-TMP	Threshold sensor CPU-1 temperature (PECI)
CPU0_DIMM0-TMP	Threshold sensor DIMM temperature (PECI)
CPU0_DIMM1-TMP	Threshold sensor DIMM temperature (PECI)
CPU0_DIMM2-TMP	Threshold sensor DIMM temperature (PECI)
CPU0_DIMM3-TMP	Threshold sensor DIMM temperature (PECI)
CPU1_DIMM0-TMP	Threshold sensor DIMM temperature (PECI)
CPU1_DIMM1-TMP	Threshold sensor DIMM temperature (PECI)
CPU1_DIMM2-TMP	Threshold sensor DIMM temperature (PECI)
CPU1_DIMM3-TMP	Threshold sensor DIMM temperature (PECI)
LAN_IO/BI-TMP	I350 LAN controller temperature
INTEGRITY	OEM integrity sensor
FMM FRU Device Locator	Add in Card FRU Device Locator (only if FMM is plugged)
FMMXXXX-TMP	FMM Temperature sensor (only if FMM is plugged)

4.3.1 Voltage Sensors

All power rails produced from +12V are monitored by the NXP LPC1768 ADC and NuvoTon NCT7904D hardware monitor devices. The ADC of LPC1768 and NCT7904D provide 8-bit resolution for voltage sensing. All the voltage sensors are listed in Table 4.4:

Sensor Name	Nominal Value	LNR	LCR	LNC	UNC	UCR	UNR
V48-CUR	range	-	-	-	7.6	8.5	9.5
HU-CAP-VOL	65	0	-	-	78	83	88
V48_A-VOL	48.0	36.0	38.0	40.0	70.0	75.0	80.0
V48_B-VOL	48.0	36.0	38.0	40.0	70.0	75.0	80.0
BAT_3_0-VOL	3.00	2.70	2.80	2.90	3.45	3.65	3.80
MAN_3_3-VOL	3.30	2.80	3.00	3.15	3.45	3.60	3.80
VSB_5_0_VOL	5.00	4.30	4.50	4.65	5.35	5.50	5.70
PAY_3_3-VOL	3.30	2.80	3.00	3.13	3.50	3.60	3.80
PAY_5_0-VOL	5.00	4.30	4.50	4.75	5.25	5.50	5.70
PAY_12-VOL	12.0	10.3	10.6	11.0	13.0	13.3	13.6
LAN_1_0-VOL	1.0	0.84	0.89	0.92	1.06	1.08	1.14
LAN_1_2-VOL	1.2	0.99	1.08	1.12	1.24	1.28	1.10
LAN_1_8-VOL	1.8	1.5	1.6	1.69	1.88	1.96	1.89
PCH_1_1-VOL	1.1	0.9	1.00	1.05	1.15	1.19	1.21
PCH_1_5-VOL	1.5	1.27	1.34	1.42	1.56	1.64	1.99
CPU0_0_85-VOL	0.85	0.75	0.79	0.85	0.95	1.00	1.40
CPU0_1_05-VOL	1.05	0.75	0.95	1.00	1.10	1.15	1.40
CPU0_CORE-VOL	1.10	0.55	-	-	-	-	1.40
CPU0_1_80-VOL	1.80	1.55	1.62	1.75	1.89	1.95	2.00
CPU1_0_85-VOL	0.85	0.75	0.79	0.85	0.95	1.00	1.40
CPU1_1_05-VOL	1.05	0.75	0.95	1.00	1.10	1.15	1.40
CPU1_CORE-VOL	1.10	0.55	-	-	-	-	1.40
CPU1_1_80-VOL	1.80	1.55	1.62	1.75	1.89	1.95	2.00
DDR_AB-VOL	1.50	1.15	1.25	1.30	1.57	1.65	1.97
DDR_CD-VOL	1.50	1.15	1.25	1.30	1.57	1.65	1.97
DDR_EF-VOL	1.50	1.15	1.25	1.30	1.57	1.65	1.97
DDR_GH-VOL	1.50	1.15	1.25	1.30	1.57	1.65	1.97

Table 4.4 MIC-5332 Voltage Sensors List

4.3.2 Thermal Sensors

Board temperatures are monitored by the NuvoTon NCT7904D, TI TMP75 and TI LM86 voltage sensors. One TMP75 (with $\pm 2^{\circ}\text{C}$ accuracy) is located in the air inlet

area and the other one is located in the air outlet area. Temperatures of the DIMM air inlet and CPU are monitored by the CPU internal digital sensor, and are read by the NCT7904D (with $\pm 1^{\circ}\text{C}$ accuracy.).

Digital error and exception events are supported by the FPGA, such as Thermal Trip, Processor Hot, DDR3 Thermal Event, and others. The management block may log thermal events and forward event messages to the Shelf Manager, or activate protection. USB ports that reside on RTM report over current alerts by the RTMLink. A CPLD on the RTM collects the signals, and forwards them to the FPGA via the RTMLink. The FPGA asserts OC#[11:8] to the PCH for alerting.

4.3.2.1 Threshold (Temperature)

The MIC-5332 supports TI TMP75 and NI LM86 as temperature sensors. When the temperature is crossing a threshold, the event will not only be logged, but the shelf manager will also adjust the system fan speed accordingly.. Advantech firmware polls all temperature sensors once per second.

Sensor Name	Value	LNR	LCR	LNC	UNC	UCR	UNR
V48-TMP	30	-5	0	5	80	90	100
INTAKE0-TMP	30	-5	0	5	65	75	85
OUTLET1-TMP	30	-5	0	5	65	75	85
PCH-TMP	30	-5	0	5	108	120	125
CPU_0-TMP	30	-5	0	5	60	65	80
CPU_1-TMP	30	-5	0	5	60	65	80
CPU0_DIMM0-TMP	30	-5	0	5	85	90	95
CPU0_DIMM1-TMP	30	-5	0	5	85	90	95
CPU0_DIMM2-TMP	30	-5	0	5	85	90	95
CPU0_DIMM3-TMP	30	-5	0	5	85	90	95
CPU1_DIMM0-TMP	30	-5	0	5	85	90	95
CPU1_DIMM1-TMP	30	-5	0	5	85	90	95
CPU1_DIMM2-TMP	30	-5	0	5	85	90	95
CPU1_DIMM3-TMP	30	-5	0	5	85	90	95
LAN_IO/BI-TMP	30	-5	0	5	80	90	95

Table 4.5 Threshold Thermal Sensors List

Note: Please refer to the FMM user manual for the FMM temperature sensors.

4.3.3 Discrete sensors

4.3.3.1 IPMC Device Locator

Each IPMC provides a PICMG compliant FRU device locator for the subsystem. This record is used to hold location and type information of the IPMC.

4.3.3.2 Mezzanine Module Device Locator

The FRU device locator for each Add-In card is also placed in the front board sensor data repository.

4.3.3.3 FRU Hotswap Sensor (Front blade)

Each IPMC contains a PICMG compliant Hot Swap sensor inside it's sensor data repository.

4.3.3.4 Version Change Sensor

A Version Change sensor is supported according to the IPMI specification.

4.3.3.5 BMC Watchdog Sensor

The BMC Watchdog sensor is supported according to the Watchdog 2 sensor type listed in the IPMI specification.

4.3.3.6 FW Progress Sensor

The IPMC SDR contains a FW Progress sensor in order to support logging of the OS boot process. The IPMC supports adding and forwarding of SEL entries from the BIOS/OS system firmware progress events by sending 'Add sel entry' commands with the matching sensor type to the IPMC through the KCS interface.

4.3.3.7 Therm Trip Sensor

The IPMC contains a sensor to monitor the CPU Therm Trip state through the FPGA on each subsystem. The sensor is implemented as a discrete OEM sensor. The single bits can be seen in following table.

Bit	7	6	5	4	3	2	1	0
Description	-	-	Memory Hot G/H	Memory Hot E/F	Memory Hot C/D	Memory Hot A/B	Therm Trip CPU 1	Therm Trip CPU 0

Table4.6: Therm Trip Sensor Bits

4.3.3.8 VR HOT Sensor

The IPMC contains a sensor to monitor the state of the voltage regulators on each subsystem. The sensor is implemented as a discrete OEM sensor. The single bits can be seen in following table.

Bit	7	6	5	4	3	2	1	0
Description	-	-	-	-	-	-	VR CPU 1 HOT	VR CPU 0 HOT

Table4.7: Voltage Regulator Sensor Bits

4.3.4 Integrity Sensor

The Integrity Sensor is an OEM sensor per IPMI specification.. It allows users to detect potential issues which are not covered by standard IPMI and/or PICMG defined sensors.

The event message of the integrity sensor contains three bytes of data. Byte 1 is the IPMI header, which is a fixed value A0. Byte 2 satisfies the component, while byte 3 stands for its action. Table 4.8 shows the supported event code structure generated by the integrity sensors on the MIC-5332:

Component	Action	Result	Byte 1	Byte 2
IPMC FW	Update	Successful	0x01	0x00
	Update	Timeout	0x01	0x04
	Update	Aborted	0x01	0x02
	Activation	Failed	0x01	0x21
	Manual Rollback	Initiated	0x01	0x15
	Automatic Rollback	Initiated	0x01	0x1D
	Rollback	Finished	0x01	0x0E
	Rollback	Failed	0x01	0x09
	Graceful Shutdown	Timeout	0x01	0x74
FPGA	Update	Successful	0x02	0x00
	Update	Timeout	0x02	0x04
	Update	Aborted	0x02	0x02
	Activation	Failed	0x02	0x21
	Manual Rollback	Initiated	0x02	0x15
	Automatic Rollback	Initiated	0x02	0x1D
	Recovery	Finished	0x02	0x0E
	Rollback	Failed	0x02	0x09

BIOS	Update	Successful	0x03	0x00
	Update	Timeout	0x03	0x04
	Update	Aborted	0x03	0x02
	Flash 0 boot	Failed	0x03	0x29
	Flash 1 boot	Failed	0x03	0x31
IPMC FRU	Common header	CKS Error	0x08	0x3B
	Internal area	CKS Error	0x08	0x43
	Chassis info area	CKS Error	0x08	0x4B
	Board info area	CKS Error	0x08	0x53
	Product info area	CKS Error	0x08	0x5B
	Multi record area	CKS Error	0x08	0x63
RTC	Time sync with ShMM	Successful	0x09	0x68
	Time sync with ShMM	Failed	0x09	0x69

Table 4.8 Integrity Sensor List

For example, below is a SEL entry generated by the integrity sensor:

```
0x0002: Event: at Jan 6 08:52:29 2010; from: (0x84,0,0); sensor: (0xc0,50); event
:0x6f(asserted): 0xA0 0x09 0x68
```

By referring to **Table 4.8, Integrity Sensor List**, this event can be interpreted as: the RTC has been successfully synced with the ShMM.

4.4 Watchdog Timers

Two kinds of watchdog timers are built into the IPMC. One is used to supervise the IPMC firmware (IPMC watchdog), and the other is used to supervise the x86 payload (BMC watchdog). When the IPMC is firmware is stuck, the IPMC watchdog bites and resets the IPMC. The payload is not affected from this watchdog event.

The BMC Watchdog of the MIC-5332 IPMC is used for:

- ◆ BIOS Power On Self Test (POST) watchdog
- ◆ OS load watchdog
- ◆ Application level watchdog (user application dependent)

After Payload power on, the BMC Watchdog will monitor the BIOS POST process and will bite in case the BIOS fails. When the watchdog bites, the payload will be reset and the IPMC selects the other BIOS image to boot. Once BIOS POST is finished successfully, the BMC watchdog timer is disabled (before the OS boot loader starts).

If the BMC watchdog is enabled again for OS load supervision, the user needs to make sure the running OS will reset or disable the BMC watchdog afterwards. If not, the IPMC will reset the payload as the timeout action.

The default timeout period for the BMC watchdog used as the BIOS POST timer and OS load supervision is 60 seconds. This setting can be changed through the BIOS setup menu. Please refer to **Section 5.6.3, Watchdog Timer Configuration**.



Note:

- ◆ To assure a safe booting process, the BMC watchdog timer cannot be set to less than 60 seconds.

4.5 E-Keying

Electronic Keying (E-Keying) is a mandatory mechanism of PICMG® 3.0 system management infrastructure, which is used to dynamically satisfy the needs that had traditionally been satisfied by various mechanical connector keying solutions:

- ◆ Prevent damage to boards
- ◆ Prevent mis-operation
- ◆ Verify fabric compatibility

4.5.1 Zone3 (RTM)

The IPMC on the MIC-5332 and the MMC on the RTM handle the E-keying control. For the RTM, the PCI Express ports need E-keying to carry out the hot swap function. Brief E-keying information of the zone 3 is listed in Table 4.10. The user may also get a detailed E-keying connectivity record via a CLI command through the shelf manager.

Channel	E-keying	Connected Source	Controlled by
Zone3 PCI Express port 0	Physical	CPU0 (Intel Xeon E5-2600) PCIe port 1	IPMC/MMC(R)
Zone3 PCI Express port 1	Physical	CPU0 (Intel Xeon E5-2600) PCIe port 0	IPMC/MMC(R)

Table 4.8 Zone 3 E-keying Information

4.6 Serial-over-LAN (SoL)

4.6.1 Overview

Serial-over-LAN (SoL) is the capability that allows establishing a remote virtual serial

console communication with the payload over a LAN interface (See **Section 4.2.1.4, NC-SI Interface**). The SoL function is available for I/O LAN (LAN1 & LAN2) and the Base Interface, but not simultaneously. Each of these two interfaces uses the Intel quad port LAN controller Intel i350-AM4, and supports the failover mechanism: As one channel in use is unexpectedly disconnected from the network, the IPMC will switch and re-establish the SoL session to the other channel within the same LAN controller automatically, to ensure the serial data in transmission will not be influenced by a link failure.

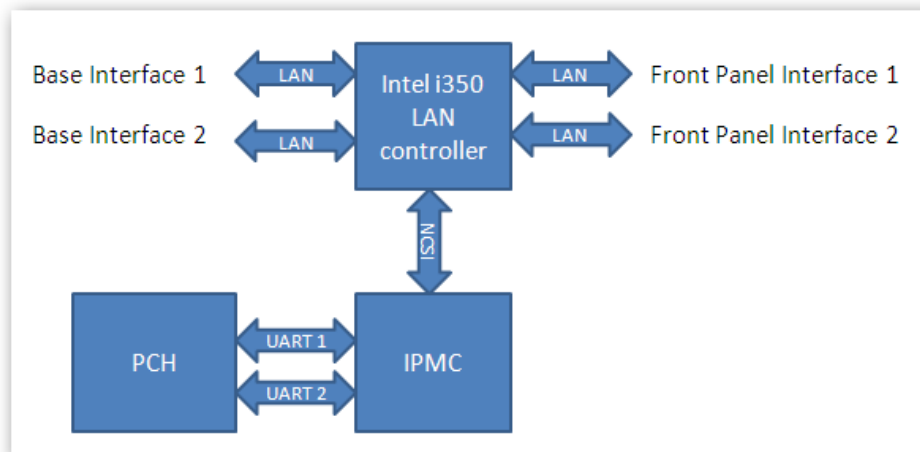


Figure 4.3 SoL Functional Block Diagram

The IPMC configures the LAN controller through the NC-SI interface and sets it in a “pass through” mode, meaning that it can send and receive Ethernet frames through the LAN controller. In this mode the GbE controller will use a dedicated MAC address to send and receive packets intended for the IPMC.

4.6.2 SoL Preparation

4.6.2.1 IPMITool

IPMITool is a utility developed to support the IPMI specification. It provides a simple command line interface, allowing users to easily establish the management application, e.g. read the FRU information, get the sensor data record, configure the LAN parameters...etc. The IPMITool utility is available in both Windows and Linux versions, and the installation procedure is described as follows:

For Windows users:

1. Open the IPMITool folder. (CD path: **\\IPMITool\\Windows**)
2. Put “cygwin1.dll”, “cygcrypto-0.9.8.dll” and “ipmitool.exe” under the same folder in the terminal PC.

3. Choose a proper connection (LAN, KCS, or IPMB) to the MIC-5332. Taking LAN for example, connect the Front Panel IO GbE-LAN RJ-45 port (LAN1 or LAN2) to the LAN port on a PC via an Ethernet cable.
4. Turn on the MIC-5332.
5. Use a command line on the remote PC, then move to the directory where IPMITool is located.
6. IPMITool is ready for use now.

For Linux users:

1. Make sure the IPMI driver has been mounted. (The built-in IPMI driver in current Linux kernel is compatible with MIC-5332)
2. Open the IPMITool folder. (CD path: **\\IPMITool\\Linux**)
3. Put "IPMITool" in a specific location on the terminal PC.
4. Follow the same procedure as Windows users from the above step 3~5.
5. IPMITool is ready for use now.

Before establishing the SoL session, the user needs to set related parameters such as user name, password, and a static IP address of LAN interface via IPMITool. The general IPMI command syntax is:

IPMITool General Command Line Syntax:

ipmitool <connection-method> <ipmitool command>

<connection-method>	The interface connected to the IPMC. User may use LAN or IPMB remotely, or KCS locally
<ipmitool command>	The command to be executed with the ipmitool

The example below shows access to the IPMC through LAN (RMCP), often referred as IPMI-over-LAN. Using KCS or IPMB is similar.

Note: If you have any problem for setup, contact Advantech technical support team.

4.6.2.2 LAN Commands

To get an overview of all possible LAN commands, please use the keyword "lan" only. If user wants to change the IP address to their need, please use the following command:

Set IP Address of the Static LAN Interface Command Line Syntax:

`ipmitool -I lan -H <ip> -A <authtype> lan set <channel> <command>
<ip address>`

-I lan	Specifies that Ethernet is used as interface for communications with the IPMC
-H <ip>	Default IP address of LAN interface 192.168.1.1
-A <authtype>	Authentication type (depending on supported types by the Shelf Manager: NONE, PASSWORD, MD2, MD5 or OEM), default: NONE
<channel>	Default used channel: 5 0: IPMB-0 1: Serial 2: unused 3: unused 4: KCS 5. LAN (default) 6: unused 7: IPMB-L
<command>	To change the IP address, please use: ipaddr
<ip address>	New IP address to be used

Example: `ipmitool -I lan -H 192.168.1.1 -A none lan set 5 ipaddr 172.21.35.105`

/ change the static IP address of LAN interface from 192.168.1.1 to 172.21.35.105 */*

4.6.3 SoL Establishment

4.6.3.1 Serial over LAN

Serial over LAN (SOL) is an extension to IPMI over LAN (IOL) and allows to transmit serial data via LAN in addition to IPMI commands (verify chapter **<x.x.x - IPMI Interfaces, LAN>**). It's defined in the IPMI v2.0 specification and based on the RMCP+ protocol to encapsulate serial data in network packets and exchange them via LAN.

With the help of SOL, user can connect to a virtual serial console (e.g. payload x86 system) from remote. SOL can be used on MIC-5332 for serial-based OS and pre-OS communication over LAN (e.g. OS command-line interface and serial redirected BIOS menu).

<1> Preconditions for SOL

<1.1> Supported LAN interfaces

Four of MIC-5332's Ethernet interfaces can be used for Serial over LAN:

- Base interface channel 1/2
- I/O interfaces 1/2

The LAN controller for NCSI is powered by management power and provides access to the management part over LAN even if payload is powered off.

<1.2> LAN Controller and UART MUX configuration

The LAN and UART configuration of the BMC is flexible and allows different configurations. To avoid "wrong" setups, users should always verify the actual LAN and UART configuration settings (chapter [<x.x.x - Configuration Setting OEM commands>](#)), before working with SOL:

- 1.) Select the LAN interface to be used (IO or Base interface)
- 2.) Make sure the LAN channel priority is appropriate
- 3.) Select OS UART interface to be used (tty0 or tty1)

<1.3> Default Parameter

Following default parameters are good to know for the initial MIC-5332 LAN setup:

IP-Address: 192.168.1.1
LAN Channel Number: 5
Username: "administrator"
Password: "advantech"

<2> LAN Configuration with IPMITool

The open source IPMITool utility is used in this chapter for the MIC-5332 SOL and LAN parameter configuration. Any other utility, based on standard IPMI commands, can be used as well.

To get an overview of all possible commands within an IPMITool command group, please use the single keywords (e.g. "lan", "user" or "sol") only.

<2.1> LAN Commands

- lan print [channel number]

Get the LAN configuration parameters for a given channel.

```
[root@localhost ~]# ipmitool lan print
Set in Progress      : Set Complete
Auth Type Support    : NONE MD5 PASSWORD
Auth Type Enable     : Callback : NONE MD5 PASSWORD
                     : User      : NONE MD5 PASSWORD
                     : Operator  : NONE MD5 PASSWORD
                     : Admin     : NONE MD5 PASSWORD
                     : OEM       :
IP Address Source    : Static Address
IP Address           : 192.168.1.1
Subnet Mask          : 255.255.255.0
MAC Address          : 00:0b:ab:3e:45:87
Default Gateway IP   : 0.0.0.0
RMCP+ Cipher Suites  : 0,1,2,3,6,7,8,11,12
Cipher Suite Priv Max : aaaaaaaaaXXXXXX
                     :      X=Cipher Suite Unused
                     :      c=CALLBACK
                     :      u=USER
                     :      o=OPERATOR
                     :      a=ADMIN
                     :      O=OEM
```

- lan set <channel> <command> [option]

This command can be used to change several IPMC LAN parameters (e.g. IP address, netmask, gateway IP address,...). Below example demonstrates how to change the IPMC IP address.

```
[root@localhost ~]# ipmitool lan set 5 ipaddr 172.21.35.104
Setting LAN IP Address to 172.21.35.104
```

<2.2> User Commands

- user list

Get the list of all supported users.

```
[root@localhost ~]# ipmitool user list
```

ID	Name	Callin	Link	Auth	IPMI Msg	Channel	Priv
1		true	true	true		CALLBACK	
2	callback	true	true	true		CALLBACK	
3	user	true	true	true		USER	
4	operator	true	true	true		OPERATOR	
5	administrator	true	true	true		ADMINISTRATOR	

- user set name <user id> [username]

This command can be used to change the user name.

```
[root@localhost ~]# ipmitool user set name 2 newuser
```

- user set password <user id> [password]

This command can be is used change the user password.

```
[root@localhost ~]# ipmitool user set password 2 newpassword
```

<3> SOL Session with IPMItool

Advantech recommends using IPMItool to successful open a SOL session with MIC-5332. The "lanplus" interface (RMCP+) of IPMItool must be used to be able to change SOL parameters and establish SOL sessions.

Following general IPMItool parameters are needed for RMCP+ and IPMItool "sol" commands:

```
ipmitool -I lanplus -H <IP-Address> -U <User> -P <Password> sol  
<SOL-Command>
```

Command Line Syntax:

-I lan	Specifies Ethernet interface
-H <IP-Address>	IP address assigned to the IPMC
-U <User>	User account, default "administrator"
-P <Password>	Password used with specified user account (default password for user "administrator" is "advantech")

<3.1> SOL Parameter Commands

- sol info [channel number]

Read out the SOL configuration parameters for a given channel.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password> sol info
Set in progress           : set-complete
Enabled                   : false
Force Encryption          : true
Force Authentication      : true
Privilege Level           : ADMINISTRATOR
Character Accumulate Level (ms) : 250
Character Send Threshold   : 32
Retry Count               : 2
Retry Interval (ms)       : 1000
Volatile Bit Rate (kbps)   : 115.2
Non-Volatile Bit Rate (kbps) : 115.2
Payload Channel           : 7 (0x07)
Payload Port              : 623
```

- sol set <parameter> <value> [channel]

This command allows modifying special SOL configuration parameters.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password> sol set
```

SOL set parameters and values:

set-in-progress	set-complete set-in-progress
commit-write	
enabled	true false
force-encryption	true false
force-authentication	true false
privilege-level	user operator admin oem
character-accumulate-level	<in 5 ms increments>
character-send-threshold	N
retry-count	N
retry-interval	<in 10 ms increments>
non-volatile-bit-rate	serial 9.6 19.2 38.4 57.6 115.2
volatile-bit-rate	serial 9.6 19.2 38.4 57.6 115.2

<3.2> SOL session activation

Finally, the IPMItool “sol activate” command need to be issued to establish the SOL session to MIC-5332 from remote.

```
# ipmitool -I lanplus <IP-Address> -U <User> -P <Password> sol activate
[SOL Session operational. Use ~? for help]
...
~. [terminated ipmitool]
```

To terminate an active IPMItool SOL session, please use the key sequence “~” + “.” (tilde and dot).

Note: There can only be one Serial over LAN session active at once!

4.7 Dynamic Power Budgeting

When the shelf manager transits the FRU to the M4 state, it will perform power budgeting based on current requirements stored in the FRU EEPROM. Instead of

replying the predefined value, e.g. 300W to the shelf manager, the MIC-5332 IPMC uses an intelligent mechanism to auto-detect current CPU type and the amount and size of the DIMMs, the RTM power draw and the FMM power draw thus calculating and reporting a power value, which is representing the real power requirements of the current blade configuration.



Note:

- ◆ The user may disable this function via Advantech's IPMI OEM command:

"ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x06 0x00 0x00".

4.8 MAC Address Mirroring

All MAC addresses consumed by the MIC-5332 will also be stored in the FRU EEPROM, making them available to be read even if the payload is not powered. User can easily get all the MAC addresses via Advantech's IPMI OEM command.

Command Line Syntax:

“Read MAC address” OEM IPMI command

Request Data

b8 00 <Command> <IANA ID> <MAC address no>

Response Data

<Completion Code> <IANA ID> <6 bytes MAC address>

Net function	0x2E / 0x2F (OEM)
<Command>	0xe2
<IANA ID>	Advantech IANA ID = 0x39 28 00
<MAC address no>	0x00 for Fabric Interface Channel 0 0x01 for Fabric Interface Channel 1 0x02 for Base Interface Channel 0 0x03 for Base Interface Channel 1 0x04 for Front Panel IO Channel 0 0x05 for Front Panel IO Channel 1 0x06 for PCH IO LAN 0x07 for FPGA NC-SI MAC (only store here) If FMM is plugged 0x08...max number of FMM MAC's – FMM MACs

Example:

```
Request    [b8 00 e2 39 28 00 00] /* read FI channel 0 MAC address */
Response   [bc 00 e2 00 39 28 00 aa bb cc dd ee ff]
           /* current MAC address: aa bb cc dd ee ff */
```

4.9 RTC Synchronization

In every ATCA system there are several different clock sources. To avoid differences in the time values, a synchronization mechanism is needed. (E.g. for timestamps of the system event logs) This feature helps to determine the master real time clock on an ATCA board. Following drawing shall give an overview of all ways to get/set the clocks. The arrows indicate the possible synchronization directions.

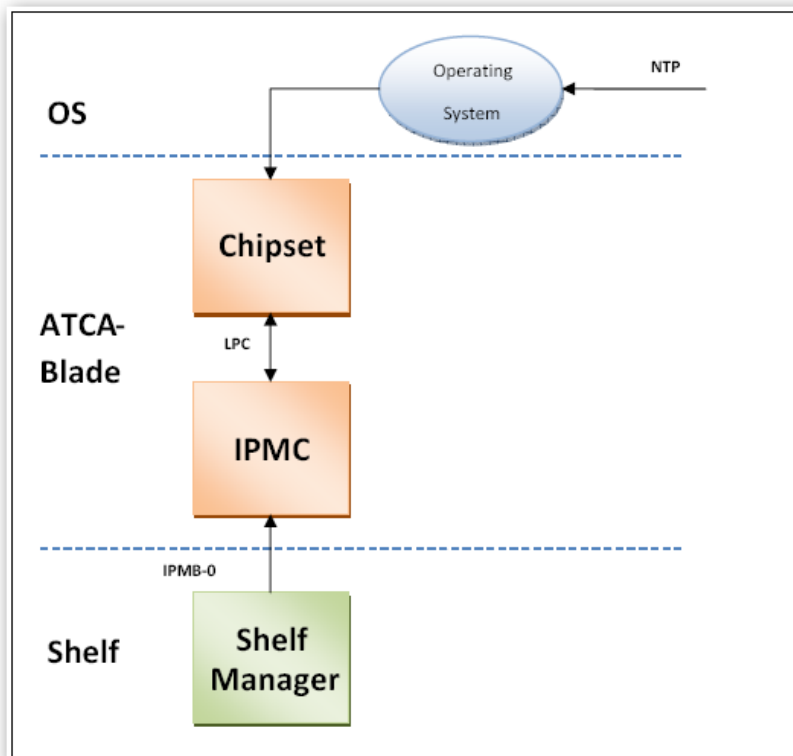


Figure 4.4 Real Time Clock Synchronization Overview

From IPMC's point of view are two more participants in an ATCA System, which maintain their own time, because they implement a separate **Real-Time-Clock**. These are the Shelf Manager and the on-board payload.

The IPMC firmware has implemented a RTC synchronization feature, which allows configuring the RTC synchronization between Shelf Manager, IPMC and payload according to the need of each user.

The IPMC will synchronize the time from Shelf Manager as soon as the ShMC is ready to communicate with the IPMC. This is done with the help of the "Get SEL Time" IPMI command.

The IPMC will do a specified number of tries to read out the Shelf Manager time. If not successful, it will generate an integrity sensor event.

IPMC synchronization with payload needs to be initiated by the payload itself (payload has to use and issue the "Get/Set SEL Time" IPMI commands). This is done by BIOS and can be performed by an OS driver via the KCS interface. IPMC is only configured to accept or not accept these commands from payload.

RTC synchronization with the ShMM is only done during the early initialization of IPMC. Synchronization with payload is always done later, after the ATCA board transitioned to M4. Means synchronization from IPMC with Shelf Manager and payload is basically independent from each other.

Chapter 5

AMI APTIO BIOS Setup

This chapter describes how to configure the AMI APTIO BIOS (UEFI BIOS).

5.1 Introduction

The AMI BIOS has been customized and integrated into many industrial and embedded motherboards for over a decade. In order to extend the features on the Intel Sandy Bridge Platform, Advantech implement the latest AMI APTIO BIOS into the MIC-5332 to enhance its operating performance.

This section describes the AMI APTIO BIOS, UEFI compliant, which has been specifically adapted to the MIC-5332. With the AMI APTIO BIOS Setup program, users can modify BIOS settings and control the special features of the MIC-5332. The setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the MIC-5332 setup screens.

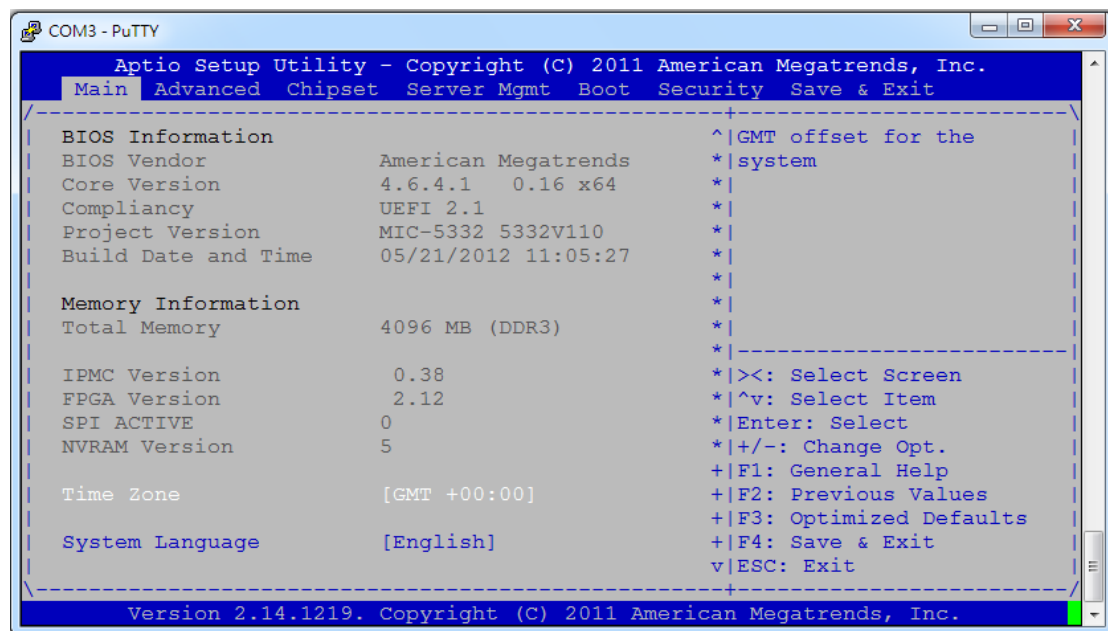


Figure 5.1 Setup Program Initial Snapshot

The BIOS has a built-in Setup program that allows users to modify the basic system configuration. There is no battery on the MIC-5332, and the integrated real-time clock is fed by IPMC management power. By using a super cap, the date and time can be kept for up to 2 hour.

5.2 Entering Setup

Turn on the computer, and there should be a POST status code displayed that

showing basic BIOS and blade information. Press or <F2> and users will immediately be allowed to enter Setup.

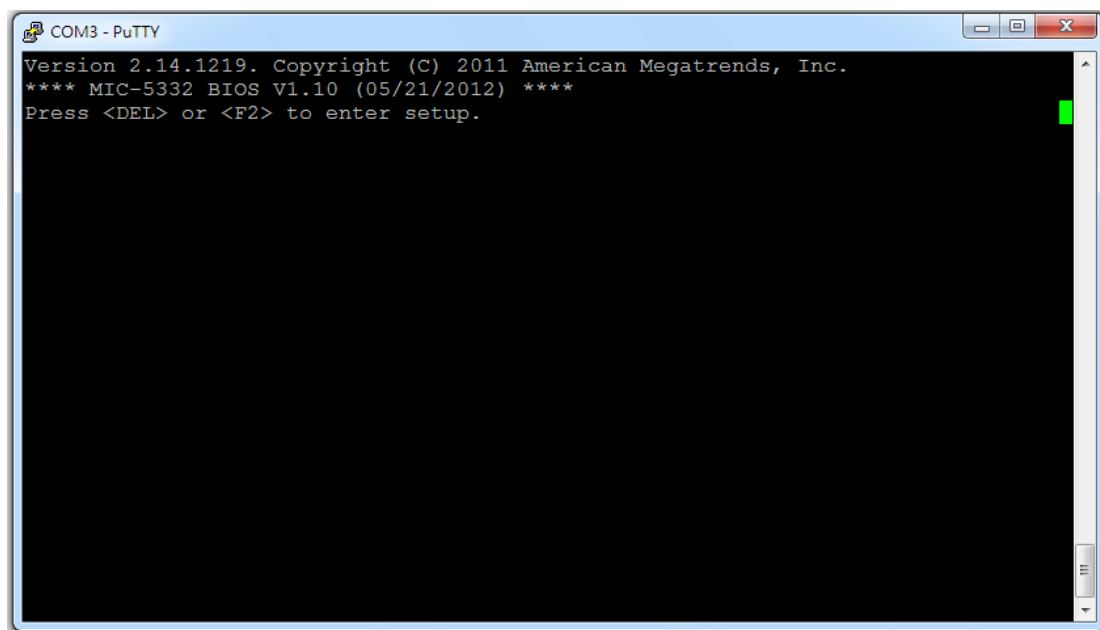


Figure 5.2 Press or <F2> to run setup

5.3 Main Setup

When users first enter the BIOS Setup Utility, users will enter the Main setup screen. Users can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message.

Feature	Default	Description
BIOS Vendor	Display only	American Megatrends
Core Version	Display only	Current BIOS core version in use
Compliance	Display only	Current UEFI version in use
Project Version	Display only	Current product name and HW version
Build Date & Time	Display only	Show board production date and time
Total Memory	Display only	Show total memories in use

IPMC Version	Display only	Show IPMC version
FPGA Version	Display only	Show FPGA version
SPI Active	Display only	Show the active SPI
Time Zone	GMT +00:00	Set the time zone
System Language	English	Set the system language
System Date	MM/DD/YY	Set the system date
System Time	HH:MM:SS	Set the system time
Access Level	Display only	Default as Administrator

Table 5.1 BIOS Menu: Main

5.3.1 Time Zone and System Language

Use this option to change the time zone and system language. Highlight Time Zone or System Language using the <Arrow> keys. Press <Enter> into the sub menu to select the correct time zone of the user location, or the proper language for further setup and maintenance.

5.3.2 System Time/ System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

5.4 Advanced BIOS Features Setup

Select the Advanced tab from the MIC-5332 setup screen to enter the Advanced BIOS Setup screen. Users can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. Users can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

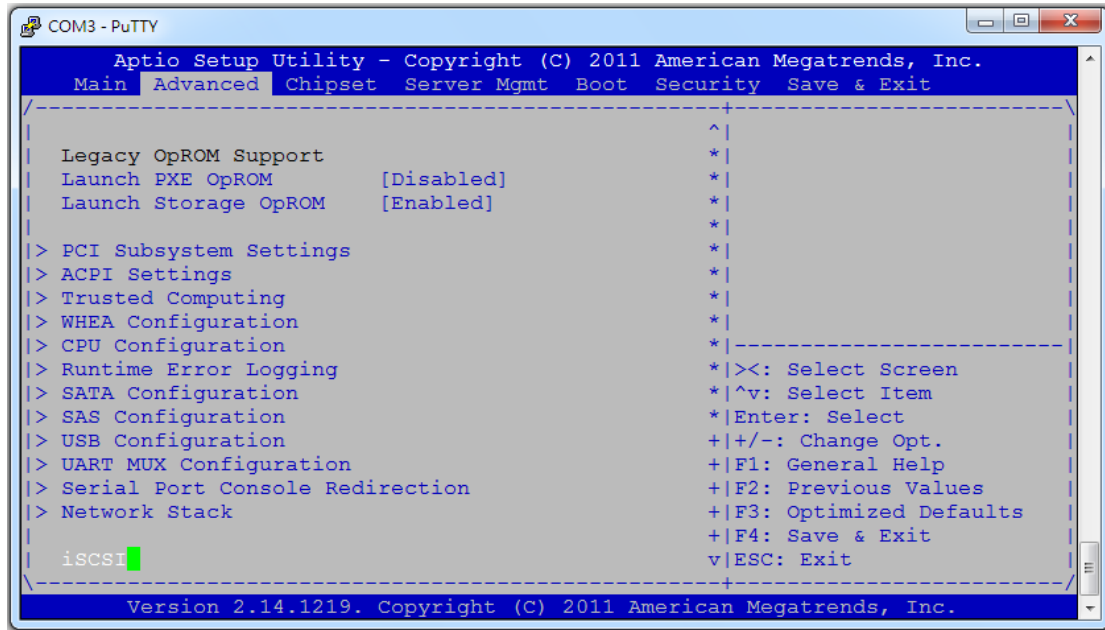


Figure 5.3 Advanced BIOS Features Setup Snapshot

Feature	Default	Description
Launch PXE OpROM	Disabled	Enable or Disable Boot Option for Legacy Network Devices
Launch Storage OpROM	Enabled	Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM
PCI Subsystem Settings	Submenu	PCI, PCI-X and PCI Express Settings
ACPI Settings	Submenu	System ACPI Parameters
Trusted Computing	Submenu	Trusted Computing Settings
WHEA Configuration	Submenu	General WHEA Configuration settings
CPU Configuration	Submenu	CPU Configuration Parameters
Runtime Error Logging	Submenu	Runtime Error Logging Support Setup Options
SATA Configuration	Submenu	SATA Devices Configuration
SAS Configuration	Submenu	SAS Devices Configuration
USB Configuration	Submenu	USB Configuration Parameters
UART MUX Configuration	Submenu	Configure UART output direction
Serial Port Console Redirection	Submenu	Serial Port Console redirection
Network Stack	Submenu	Network stack Settings
iSCSI	Submenu	Set the worldwide unique name of the initiator.
Main Configuration Page	Submenu	Click to configure the network device ports.

Table 5.2 BIOS Menu: Advanced Setting

5.4.1 PCI Subsystem Settings

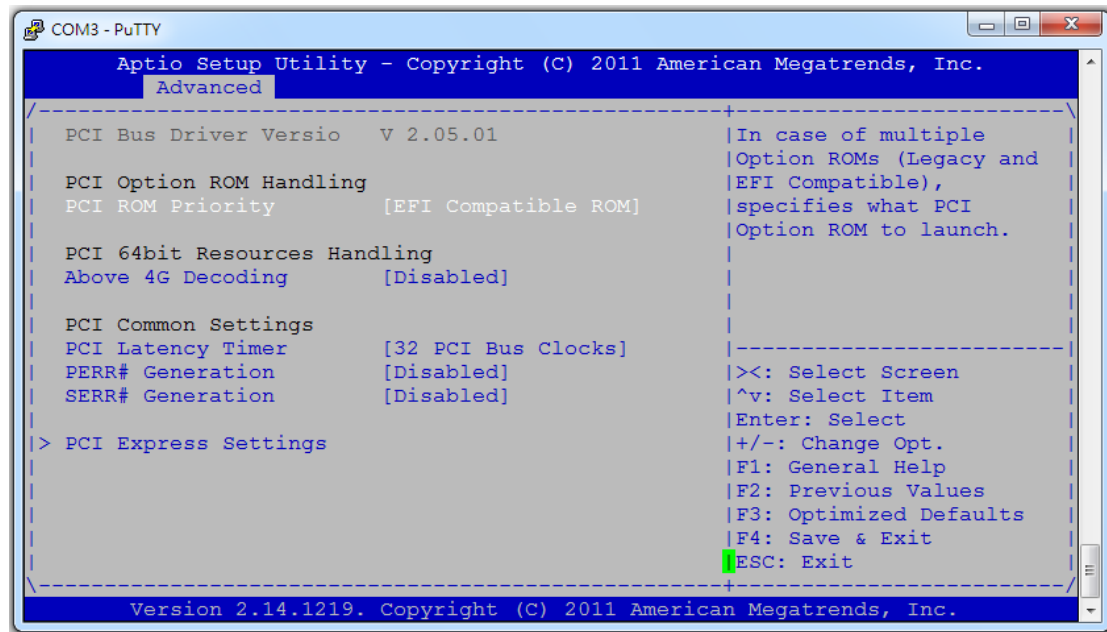


Figure 5.4 PCI Subsystem Settings

Feature	Default	Description
PCI Bus Driver Version	Display only	Show current PCI bus driver version
PCI ROM Priority	EFI Compatible ROM	In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.
Above 4G Decoding	Disabled	Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).
PCI Latency Timer	32 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register.
PERR# Generation	Disabled	Enables or Disables PCI Device to Generate PERR#.
SERR# Generation	Disabled	Enables or Disables PCI Device to Generate SERR#.
PCI Express Settings	Submenu	Change PCI Express Devices Settings.

Table 5.3 PCI Subsystem Settings

5.4.1.1 PCI Express Settings

Users can enter in the submenu of PCI Express Settings to setup the Maximum Payload (default as auto) and Maximum Read Request (default as auto).

5.4.2 ACPI Settings

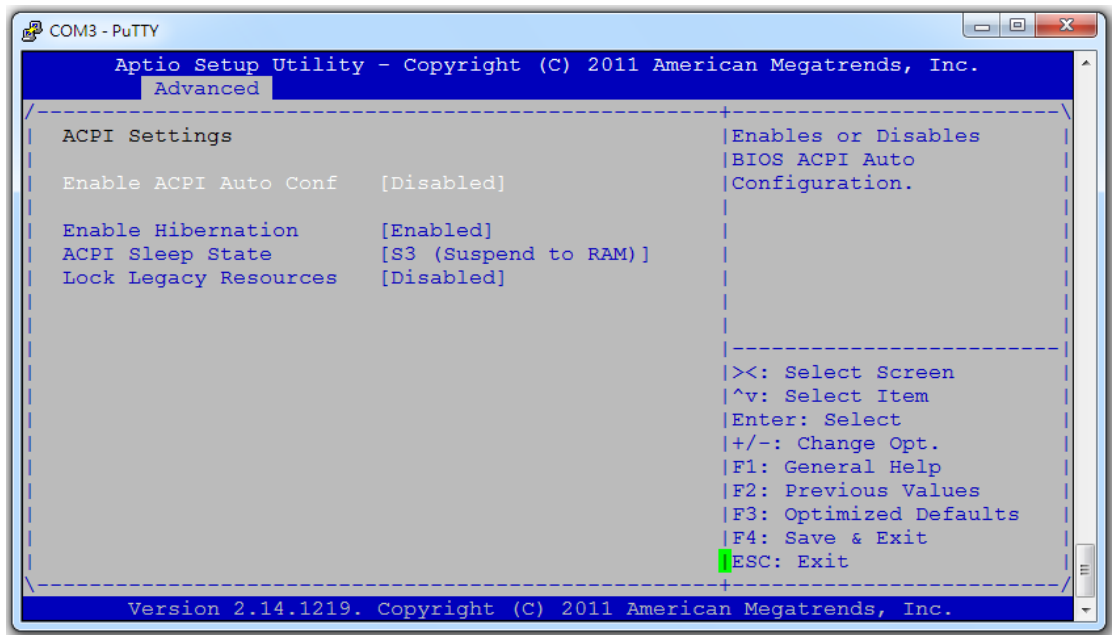


Figure 5.5 ACPI Settings

Feature	Default	Description
Enable ACPI Auto Conf	Disabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Enabled	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	S3 (Suspend to RAM)	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy Resources	Disabled	Enables or Disables Lock of Legacy Resources.

Table 5.4 ACPI Settings

5.4.3 Trusted Computing

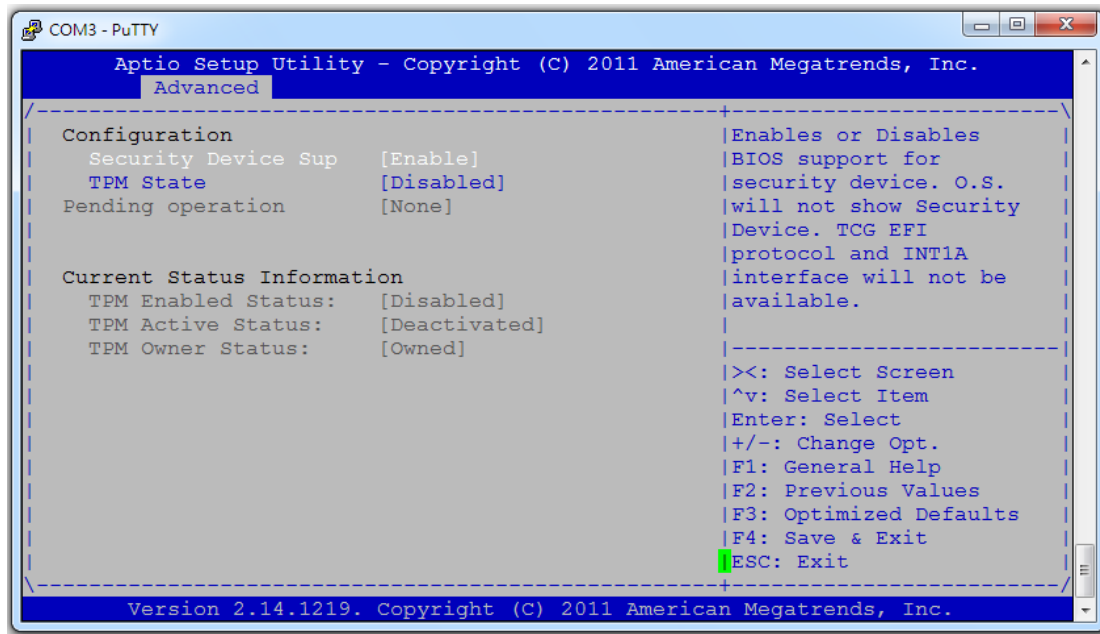


Figure 5.6 Trusted Computing

Feature	Default	Description
Security Device Sup	Enabled	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
TPM State	Disabled	Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.
Pending Operation	Display Only	Show current pending operation item.
TPM Enabled Status	Display Only	Show current enabled status.
TPM Active Status	Display Only	Show current active status.
TPM Owner Status	Display Only	Show current owner status.

Table 5.5 Trusted Computing

5.4.4 WHEA Configuration

The user can enable or disable the Windows Hardware Error Architecture (WHEA) support via a sub option of advanced setting (the default is disabled).

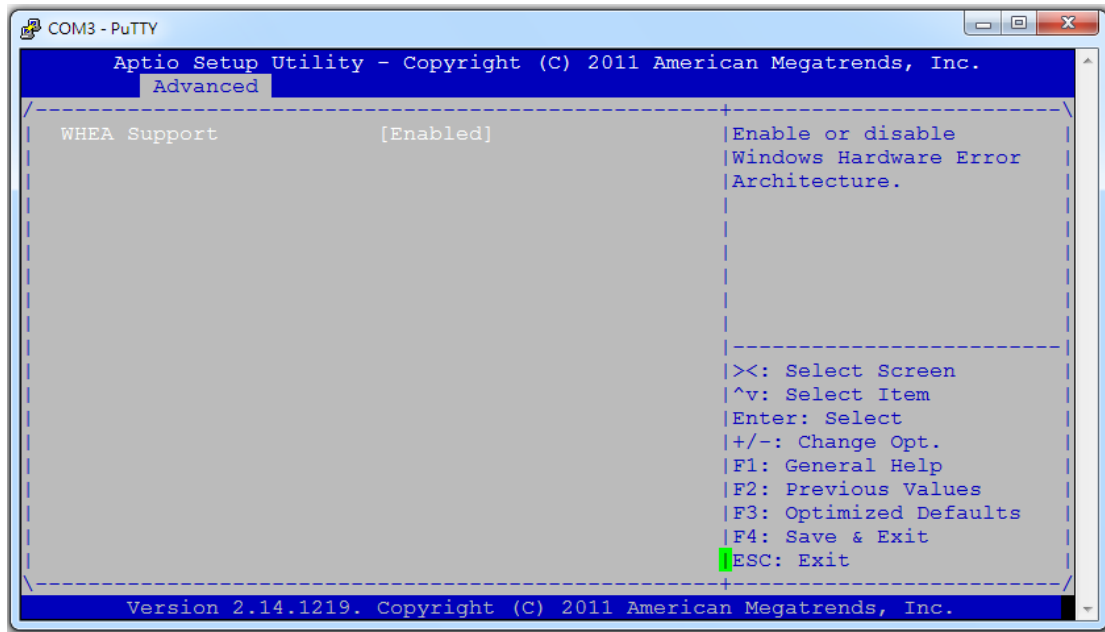


Figure 5.7 WHEA Configuration

5.4.5 CPU Configuration

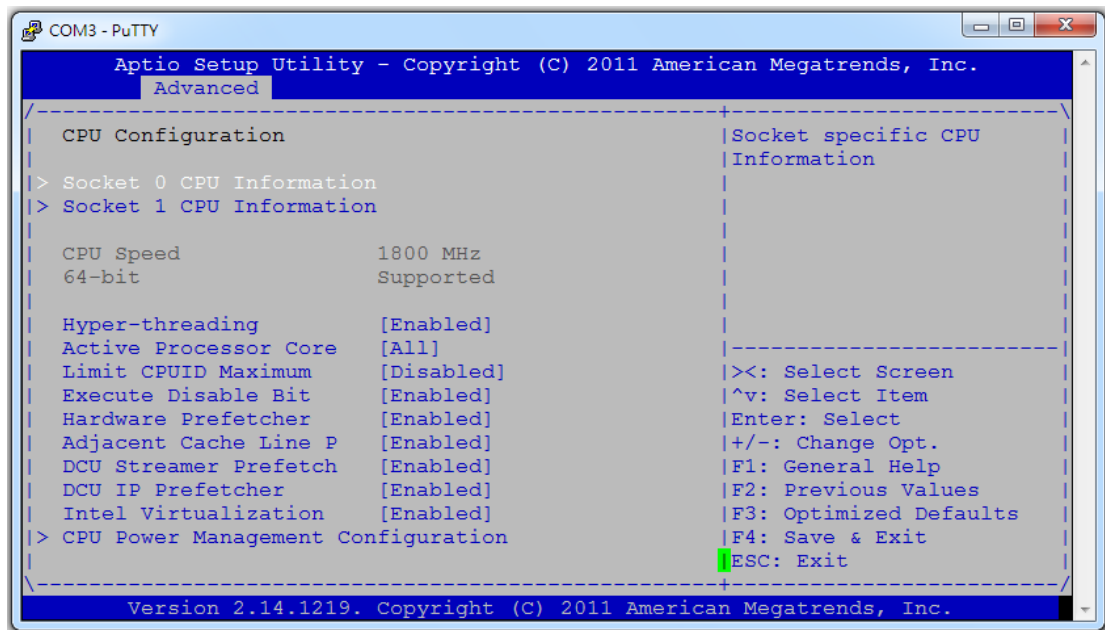


Figure 5.8 CPU Configuration

Feature	Default	Description
Socket 0 CPU Information	Display Only	Socket specific CPU Information
Socket 1 CPU Information	Display Only	Socket specific CPU Information
CPU Speed	Display Only	Show the current CPU speed in use

64-bit	Display Only	Show if the current CPU supports 64-bit or not
Hyper-threading	Enabled	Enabled for Windows XP and Linux (OS optimized for HT Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one.
Active Processor Core	All	Number of cores to enable in each processor package.
Limit CPUID Maximum	Disabled	Disabled for Windows XP
Execute Disable Bit	Enabled	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)
Hardware Prefetcher	Enabled	Enable the Mid Level Cache (L2) streamer prefetcher.
Adjacent Cache Line P	Enabled	Enable the Mid Level Cache (L2) prefetching of adjacent cache lines.
DCU Streamer Prefetcher	Enabled	Enable prefetch of next L1 Data line based upon multiple loads in same cache line.
DCU IP Prefetcher	Enabled	Enable prefetch of next L1 line based upon sequential load history.
Intel Virtualization	Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
CPU Power Management Configuration	Submenu	CPU Power Management Configuration Parameters

Table 5.6 CPU Configuration

5.4.5.1 CPU Power Management Configuration

Users can enter into the submenu to configure CPU power management. The user can get the CPU frequency ratio info, CPU power consumption info and CPU long duration info from this configuration. Also, they can select (defined) or adjust (custom) the proper parameters to handle the power management for system performance enhancement or power saving.

5.4.6 Runtime Error Logging

User can enable or disable the runtime error logging support via a sub option of the advanced setting (default is disabled).

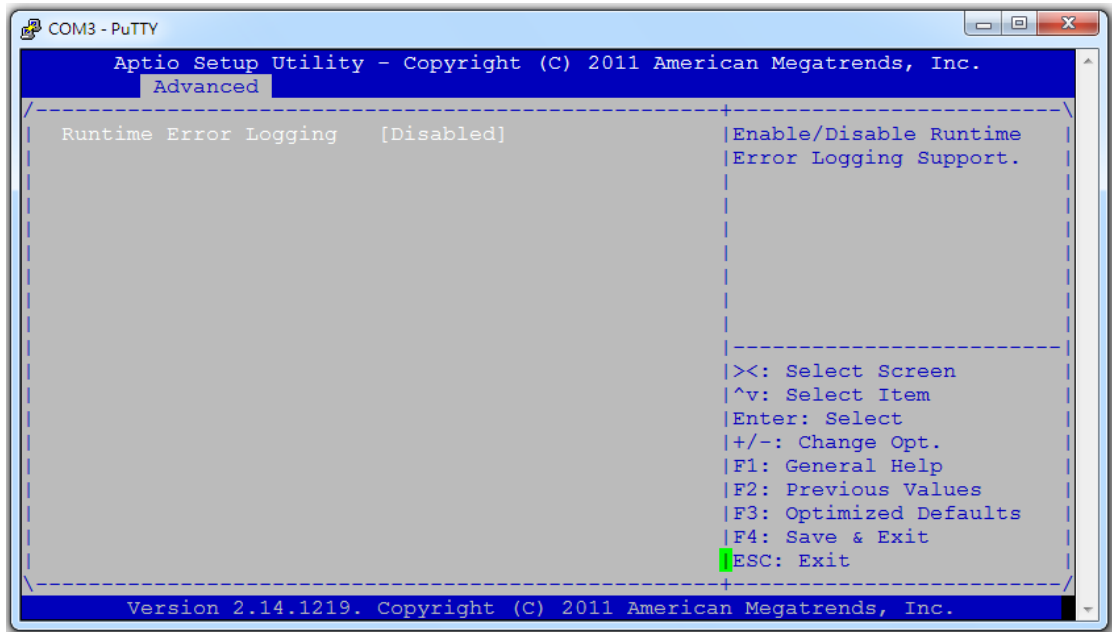


Figure 5.9 Runtime Error Logging

5.4.7 SATA Configuration

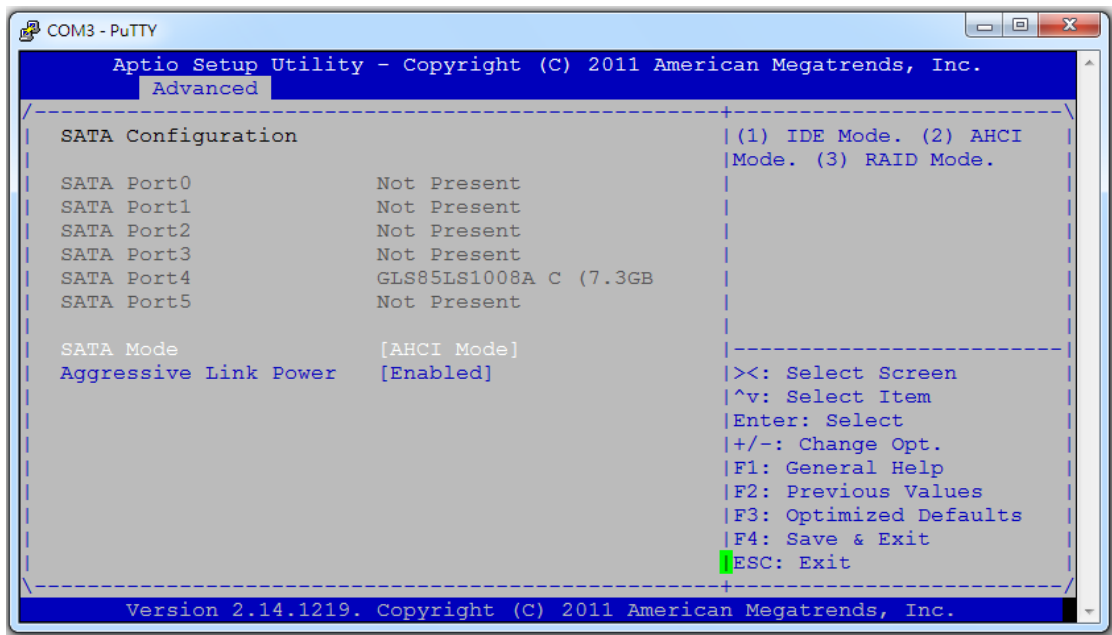


Figure 5.10 SATA Configuration

Feature	Default	Description
SATA Port0	Display only	Show current SATA devices in use on the MIC-5332
SATA Port1	Display only	
SATA Port2	Display only	
SATA Port3	Display only	
SATA Port4	Display only	
SATA Port5	Display only	
SATA Mode	AHCI Mode	(1) IDE Mode. (2) AHCI Mode. (3) RAID Mode.
Aggressive Link Power	Enabled	Aggressive Link Power Management Support.

Table 5.7 SATA Configuration

The MIC-5332 supports total 6 SATA devices (details, please refer to section 2.2.6). Users can check the status each by each via this sub option. Also users can select the proper SATA mode to guide the operation system when SATA devices are plugged on the MIC5332.

5.4.8 SAS Configuration

The MIC-5332 supports total 4 SAS devices (details, please refer to section 2.2.6). Users can check each status via this sub option.

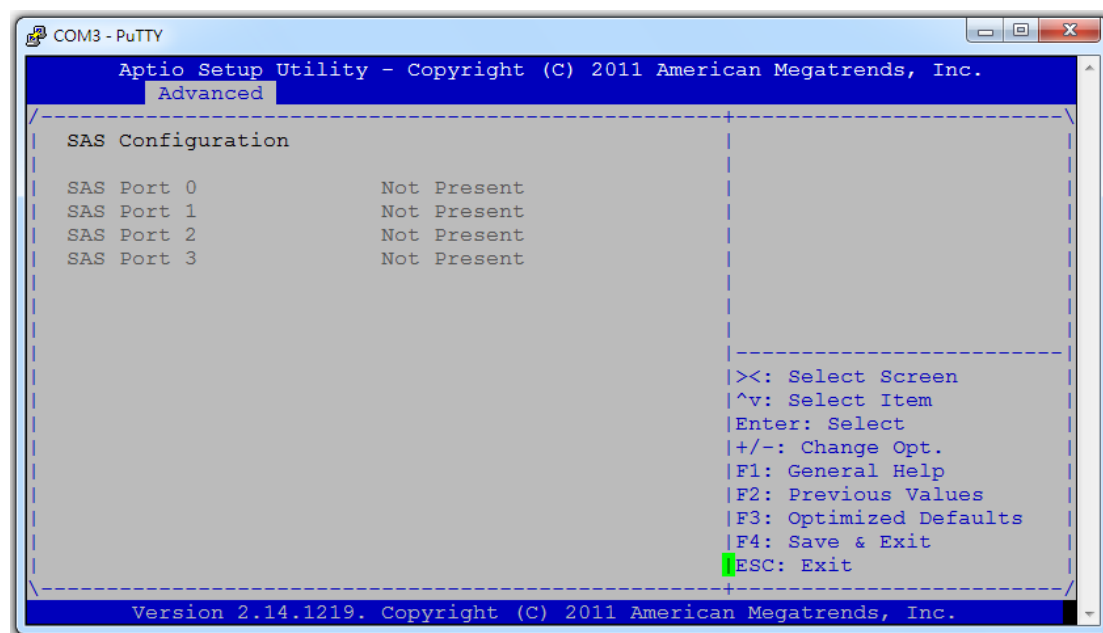


Figure 5.11 SAS Configuration

5.4.9 USB Configuration

The MIC-5332 supports USB Plug & Play, PnP. That is, users can find all USB devices which are plugged on the MIC-5332. They can configure the parameters to enhance the USB device performance, such as mass storage devices.

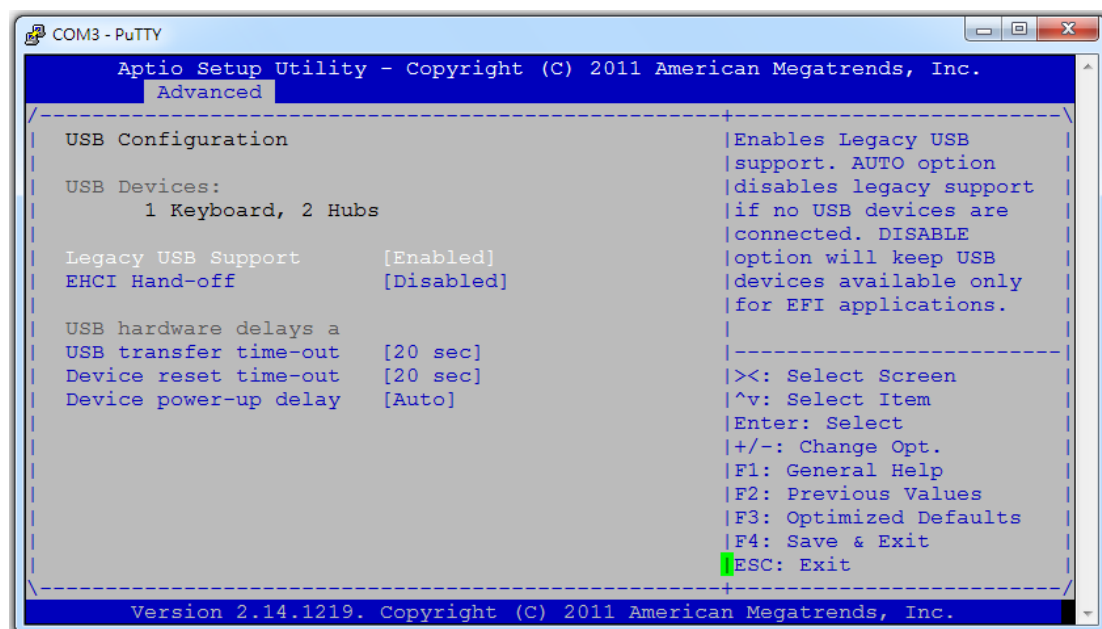


Figure 5.12 USB Configuration

Feature	Default	Description
Legacy USB Support	Enabled	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI application.
EHCI Hand-off	Disabled	This is a workaround for OSES without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.
USB transfer time-out	20 sec	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	20 sec	USB mass storage device Start Unit command time-out.
Device power-up delay	Auto	Maximum time the device will take before it properly reports itself to the Host Controller. 'AUTO' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

Table 5.8 USB Configuration

5.4.10 UART MUX Configuration

The MIC-5332 supports two UART channels. Users can select the different methods (SoL, FP-RJ45, FP-USB, RTM0 and RTM1) to access the UART channel. The default setting for channel1 is FP-USB, and FP-RJ45 for channel2. Users can also decide to open all available methods to access the UART channel.

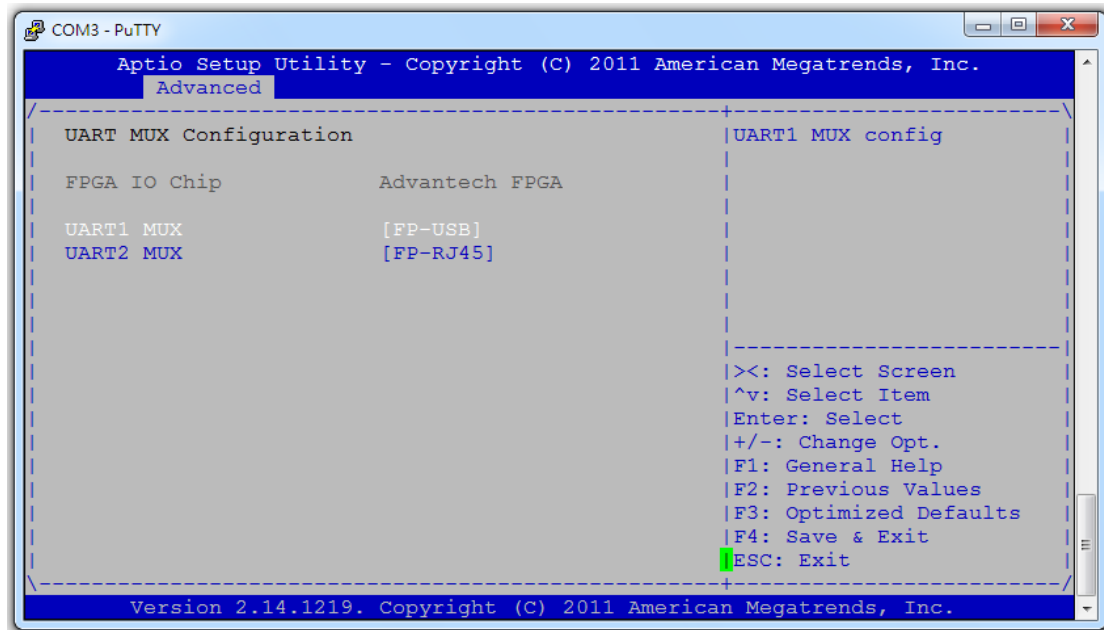


Figure 5.13 UART MUX Configuration

5.4.11 Serial Port Console Redirection

The MIC-5332 has two COM ports that are integrated on the front panel. One is COM1 through the RJ45 connector, and another is COM2 through the miniUSB connector. Users can configure the related parameters of these two serial port consoles in this submenu. For example, users can define the terminal type, bits per second, data bits, parity, stop bits and others for each serial port console.

Feature	Default	Description
Console Redirection	Enabled	Console Redirection Enable or Disable.
Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
Console Redirection	Enabled	Console Redirection Enable or Disable.

Console Redirection Settings	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
------------------------------	---------	--

Table 5.9 Serial Port Console Redirection

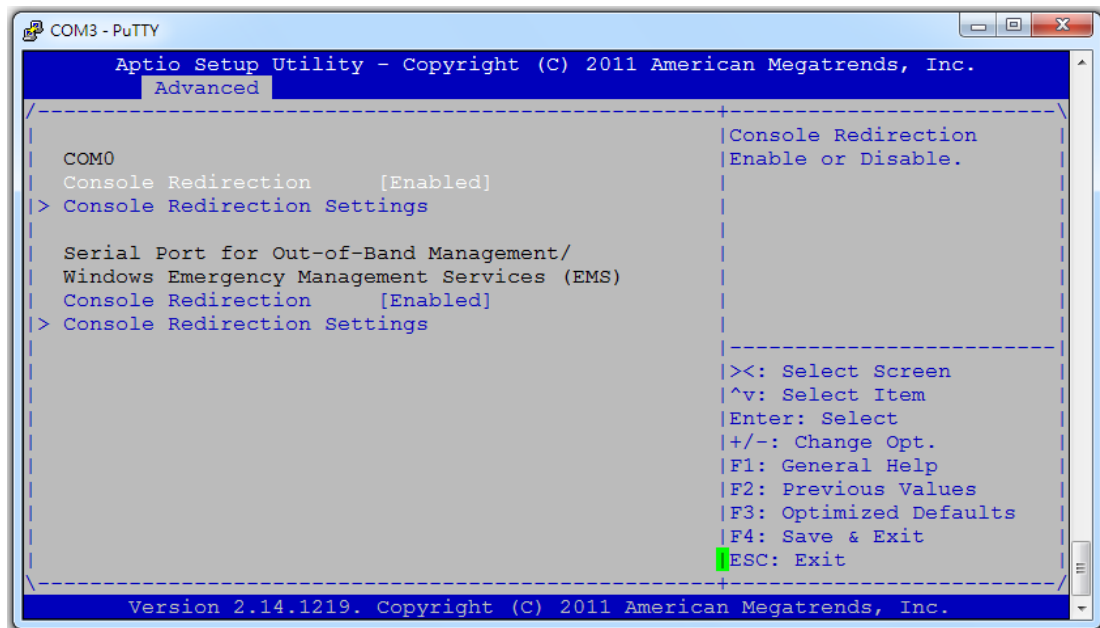


Figure 5.14 Serial Port Console Redirection

5.4.12 Network Stack

Users can enable or disable the network stack (PXE and UEFI) via this submenu (default is disable Link).

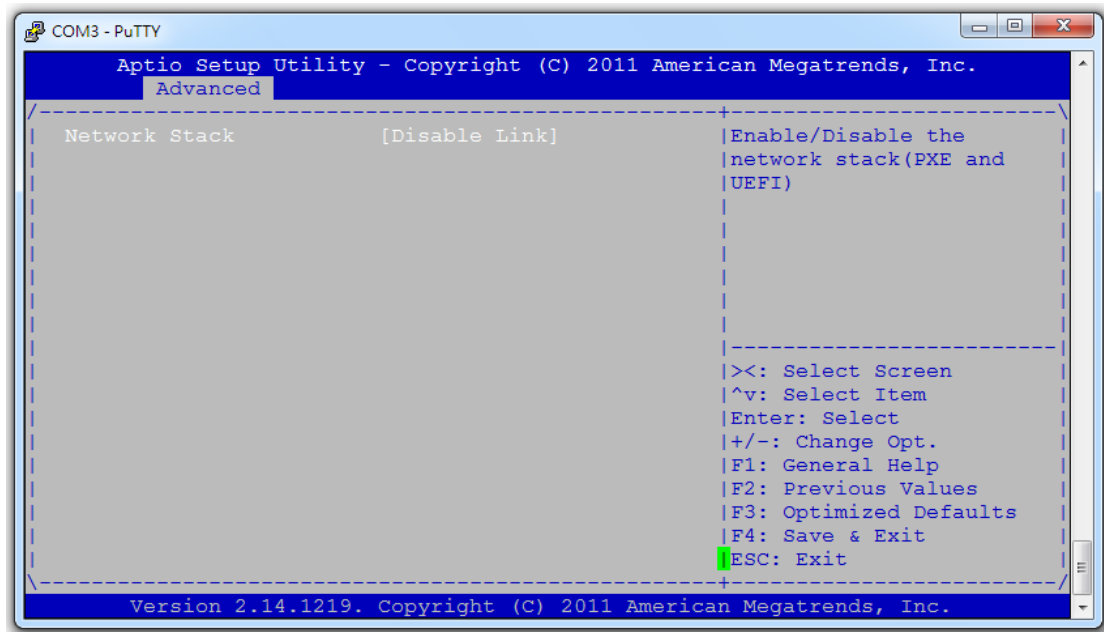


Figure 5.15 Network Stack

5.4.13 iSCSI

This function allows users to give a worldwide unique name for the iSCSI initiator.

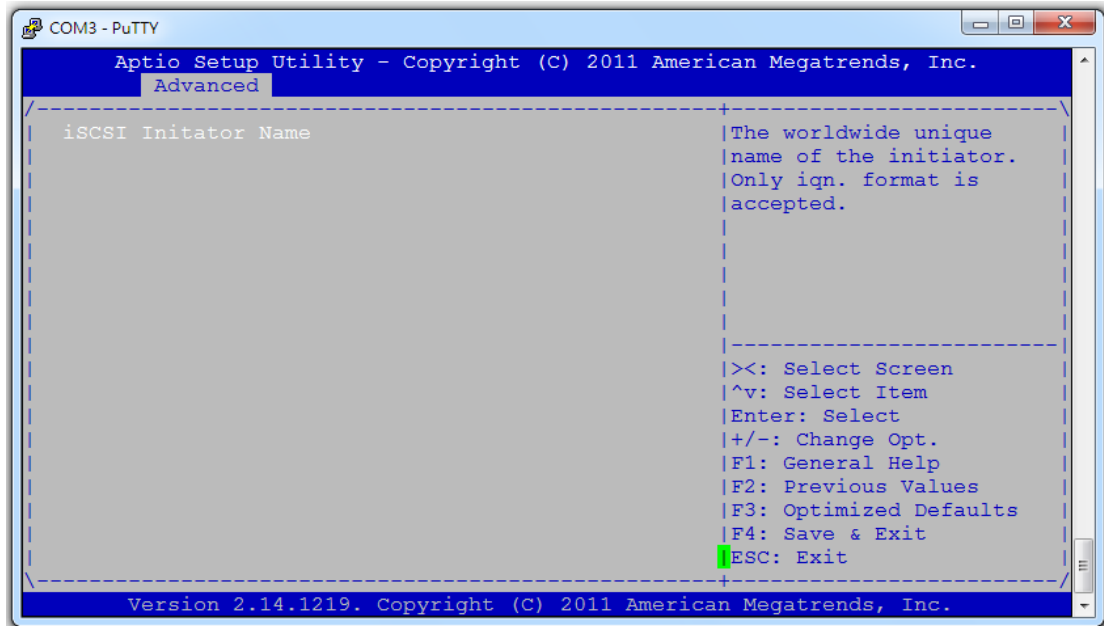


Figure 5.16 iSCSI Initiator

5.4.14 Main Configuration Page

The MIC-5332 supports five MACs (four from the Intel i350, one from the PCH). Users can configure legacy boot protocol, link speed and Wake On LAN for each of them.

Also, users can find the corresponding MAC address for each LAN here.

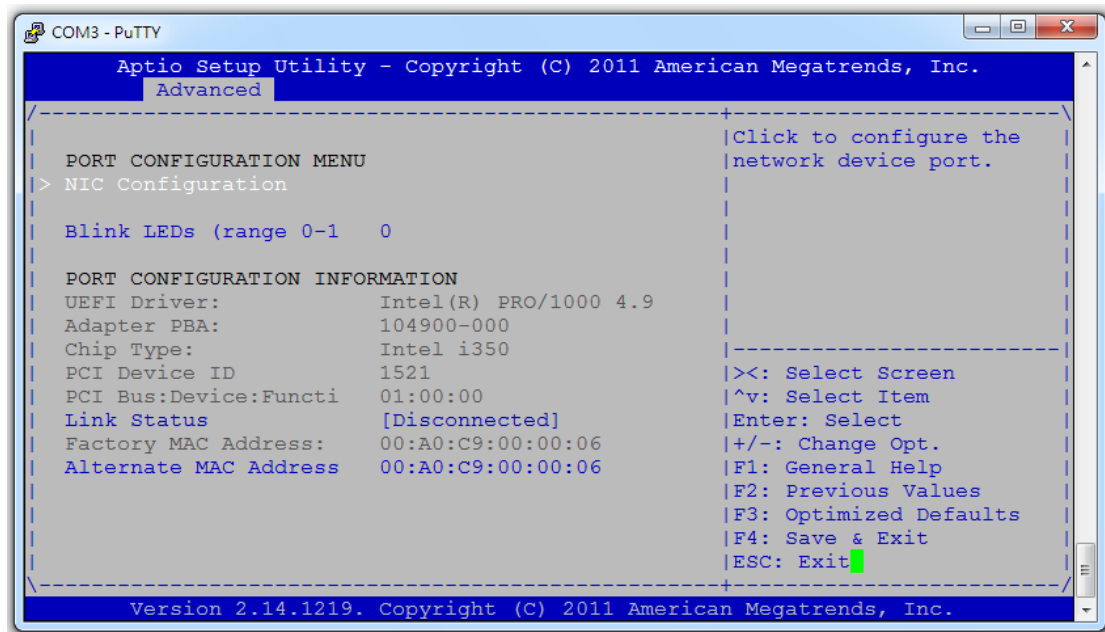


Figure 5.17 Main Configuration Page

5.5 Chipset Setup

Select the chipset tab from the MIC-5332 setup screen to enter the Chipset Setup screen. Users can configure the parameters of north bridge (CPU), south bridge (PCH) and ME system (display only), respectively.

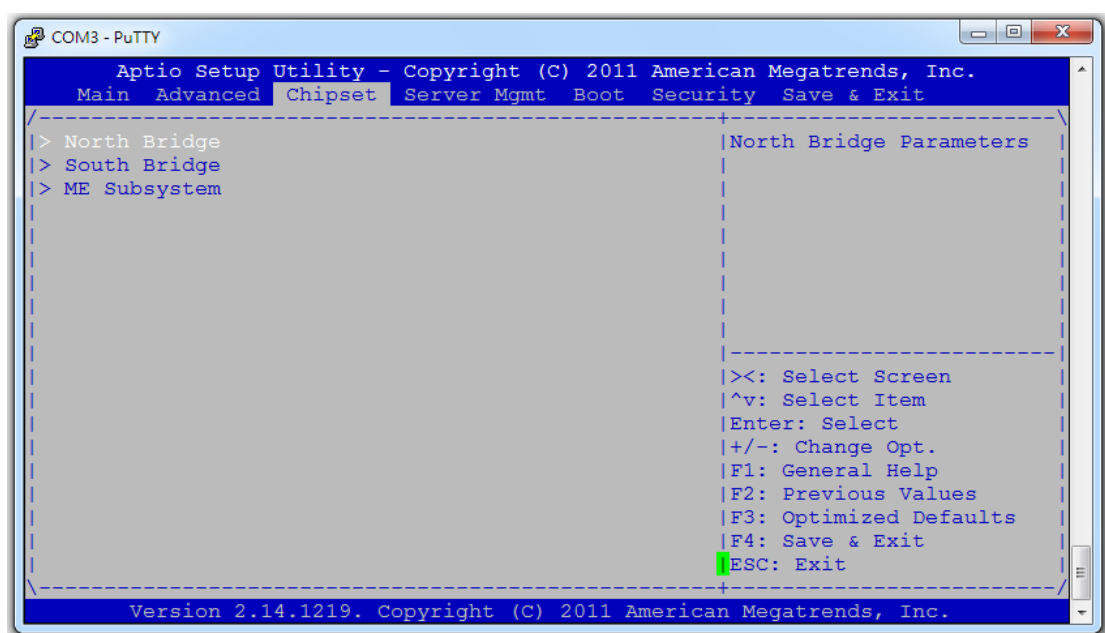


Figure 5.16 Chipset Configuration

5.5.1 North Bridge

Users can set up all parameters related to the IOH function in the North Bridge page. Moreover, the MIC-5332 BIOS allows users to configure the PCIe link speed (gen1, gen2 or gen3) and its functions visible (x16, x8x8, x8x4x4, x4x4x8 or x4x4x4x4) in the IOH configuration submenu. Also, the Sandy Bridge CPU supports two QPI channels. Users can configure the related settings in the QPI configuration submenu.

Feature	Default	Description
IOH Configuration	Submenu	IOH Configuration Page
QPI Configuration	Submenu	QPI Configuration Page
Compatibility RID	Enabled	Support for Compatibility Revision ID (CRID) Functionality mentioned in Sandy Bridge Bios spec
Total Memory	Display only	Show total memory capacity
Current Memory Mode	Display only	Show current memory mode
Current Memory Speed	Display only	Show current memory speed
Mirroring	Display only	Show mirroring status
Sparing	Display only	Show Sparing status
Memory Mode	Independent	Select the mode for memory initialization.
NUMA	Enabled	Enable or Disable Non uniform Memory Access.
DDR Speed	Auto	Force DDR Speed
Channel Interleaving	Auto	Select different Channel Interleaving setting.
Rank Interleaving	Auto	Select different Rank Interleaving setting.
Patrol Scrub	Enabled	Enable/Disable Patrol Scrub
Demand Scrub	Disabled	Enable/Disable Demand Scrubbing Feature
Data Scrambling	Disabled	Enable/Disable Data Scrambling.
Device Tagging	Disabled	Enable/Disable Device Tagging.
DIMM Information	Display Only	Show current DIMMs status in use.

Table 5.10 North Bridge Configuration

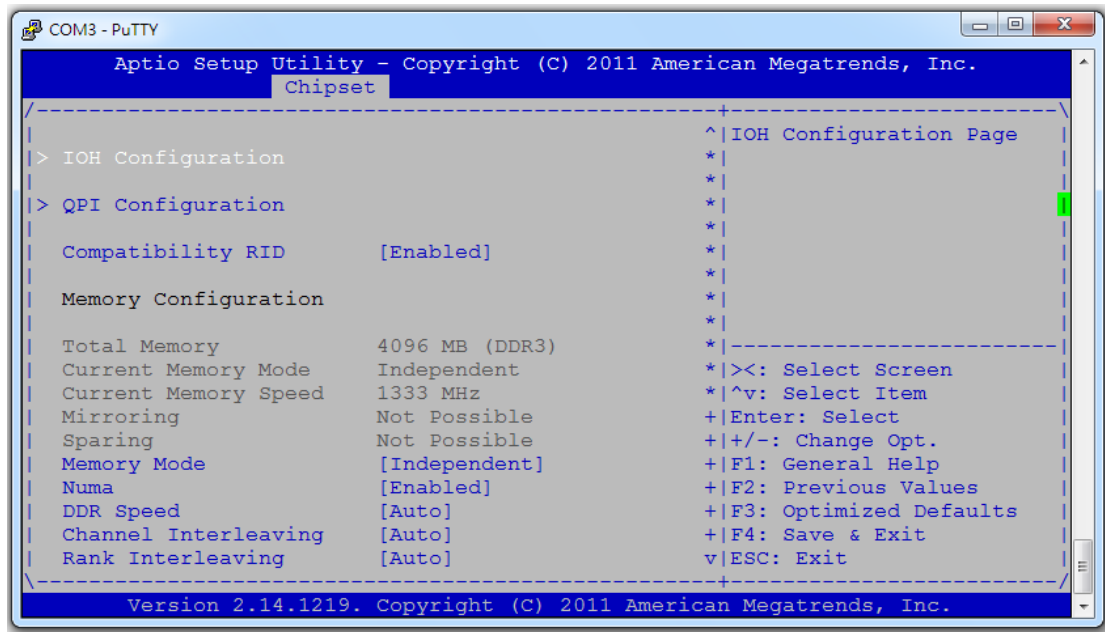


Figure 5.17 North Bridge Configuration

5.5.2 South Bridge

Users can set up all parameters related to the PCH function in the South Bridge page. Also, users can configure (to enable or disable) eight USB 2.0 channels supported on the MIC-5332 in this page.

Feature	Default	Description
Name	Display only	
Stepping	Display only	
PCH Compatibility RID	Disabled	Support for PCH Compatibility Revision ID (CRID) Functionality.
SMBus Controller	Enabled	Enabled/Disabled SMBus Controller.
GbE Controller	Enabled	Enabled/Disabled GbE Controller.
Wake on Lan from S5	Enabled	Enabled/Disabled GbE control PME in S5.
SLP_S4 Assertion Stre	Enabled	Enabled/Disabled SLP_S4# Assertion Stretch.
SLP_S4 Assertion Wid	4-5 Seconds	Select a minimum assertion width of the SLP_S4# signal.
Deep Sx	Disabled	Deep Sx configuration. NOTE: Mobile platforms support Deep S4/S5 in DC only and Desktop platforms support Deep S4/S5 in AC only.

Disable SCU devices	Disabled	Enable/Disable Patsburg SCU Devices.
Onboard SAS Oprom	Disabled	Enable/Disable onboard SAS Option rom if Launch Storage OpROM is enabled.
Onboard SATA RAID Opr	Enabled	Enable/Disable onboard SATA RAID Option rom if Launch Storage OpROM is enabled.
High Precision Timer	Enabled	Enable/Disable the High Precision Event Timer.
USB Configuration	Submenu	Advanced USB Configuration

Table 5.11 South Bridge Configuration

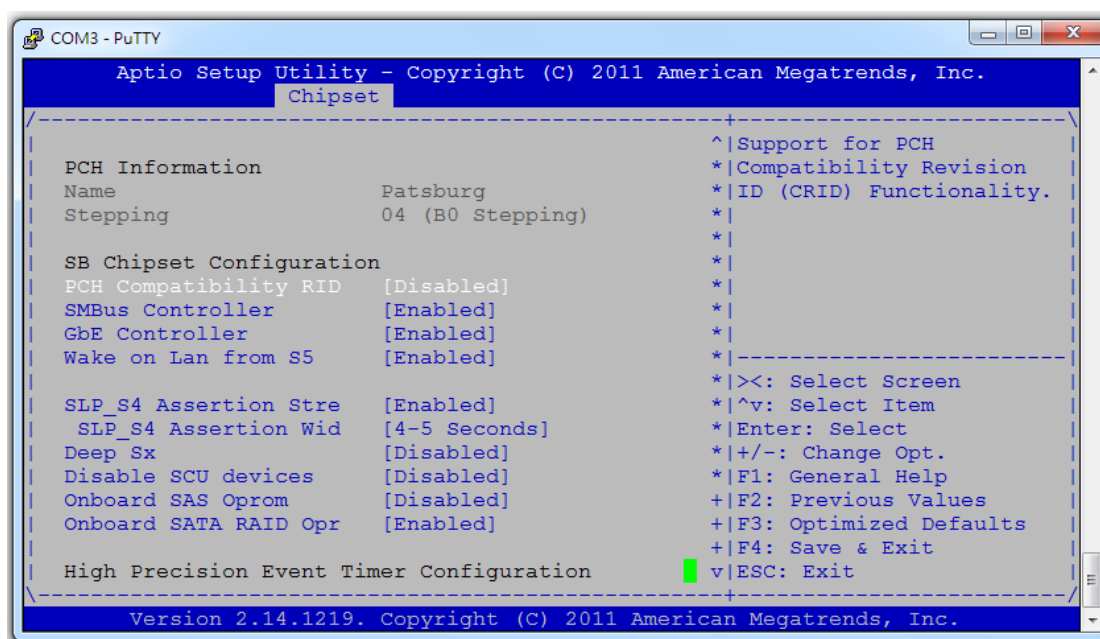


Figure 5.18 South Bridge Configuration

5.6 Server Management (Mgmt) Setup

Users can configure the watchdog timer both for the FRB-2 and OS Wtd in the server mgmt page. For details of the BMC self test log and system event log, users can decide to enable the function to record the logs, or erase the logs through BMC self test log submenu, or the system event log submenu. Also, users can check the FRU information via the submenu of view FRU information (display only).

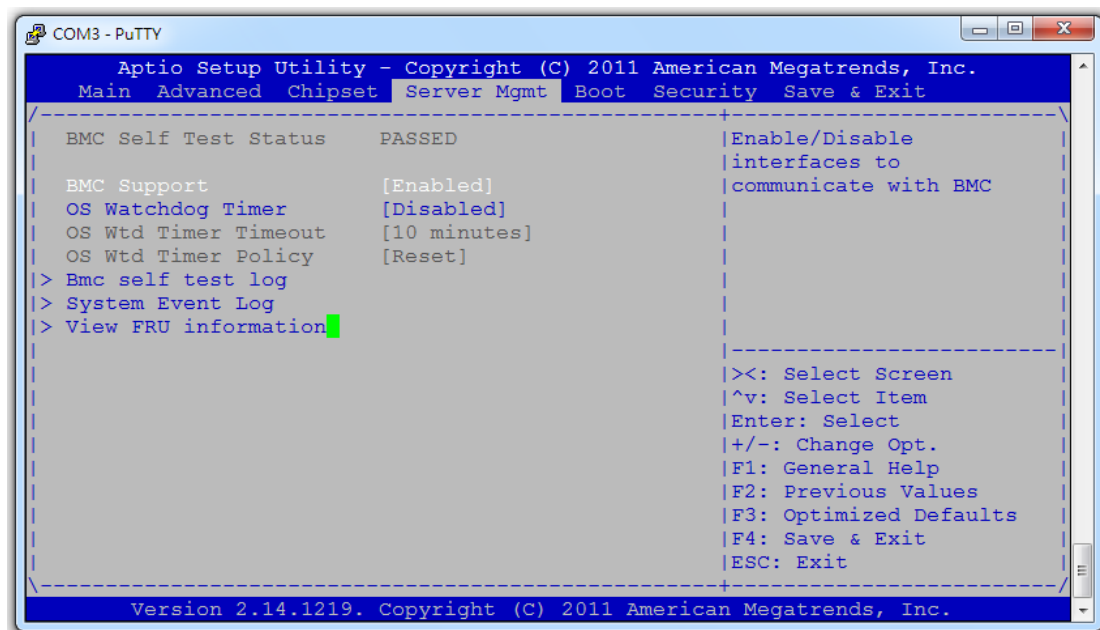


Figure 5.19 Server Mgmt Configuration

Feature	Default	Description
BMC Support	Enabled	Enable/Disable interfaces to communicate with the BMC.
OS Watchdog Timer	Disabled	If enabled, starts a BIOS timer which can only be shut off by Intel Management Software after the OS loads. Helps determine that the OS successfully loaded or follows the OS Boot.
OS Wtd Timer Timeout	10 minutes	Configure the length of the OS Boot Watchdog Timer. Not available if OS Boot Watchdog Timer is disabled.
OS Wtd Timer Policy	Reset	Configure how the system should respond if the OS Boot Watchdog Timer expires. Not available if OS Boot Watchdog Timer is disabled.

BMC self test log	Submenu	Logs the report returned by the BMC self test command.
System Event Log	Submenu	Press <Enter> to change the SEL event log configuration.
View FRU information	Display Only	Press <Enter> to view FRU information.

Table 5.12 Server Mgmt Configuration

5.7 Boot Setup

Users can configure the system boot priority settings via the boot page. The default setting of boot priority of boot option #1 is “Disabled in BBS Order”; option #2 is “UEFI: Built-in EFI Shell”; and option #3 is “Windows Boot Manager.” Users can define the boot priorities based on the application.

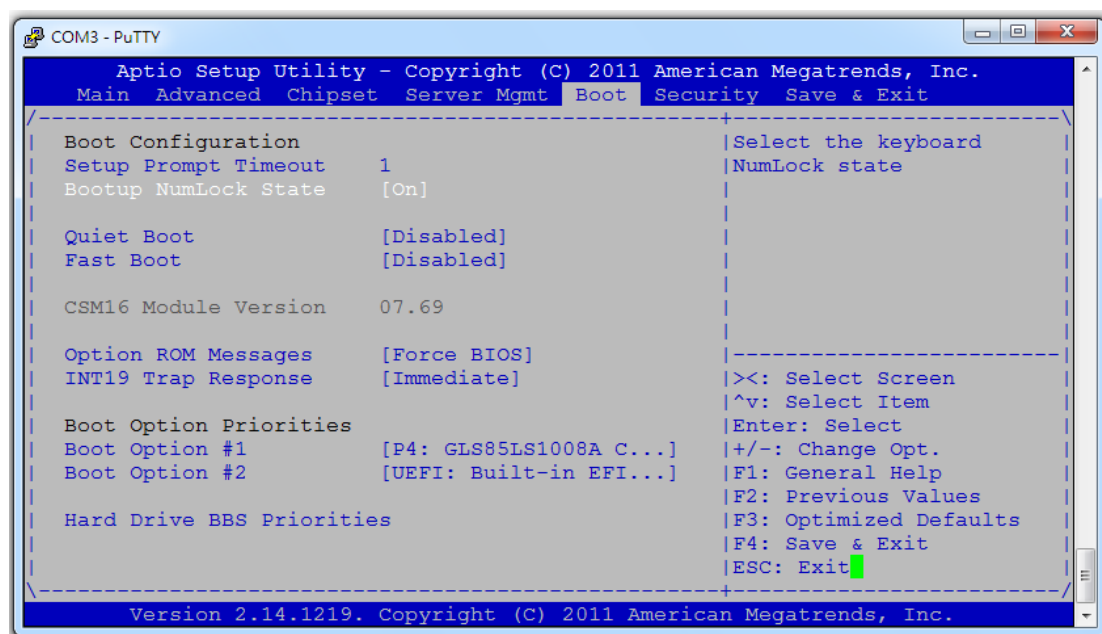


Figure 5.20 Boot Configuration

Feature	Default	Description
Setup Prompt Timeout	1	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	On	Select the keyboard NumLock state.
Quiet Boot	Disabled	Enables or disables Quiet Boot option.

Fast Boot	Disabled	Enables or disables boot with an initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot option.
CSM16 Module Version	Display Only	Shows the current version in use.
Option ROM Messages	Force BIOS	Set display mode for Option ROM.
Interrupt 19 Capture	Immediate	Enabled: Allows Option ROMs to trap Int 19.
Boot Option	User Defined	Sets the system boot order.
Hard Drive BBS Priorities	Submenu	Set the order of the legacy devices in this group.

Table 5.13 Boot Configuration

5.8 Security Setup

The two items “**Administrator Password**” and “**User Password**” allow users to configure the system so that a password after being installed is required each time the system boots, and/or an attempt is made to enter the Setup program.

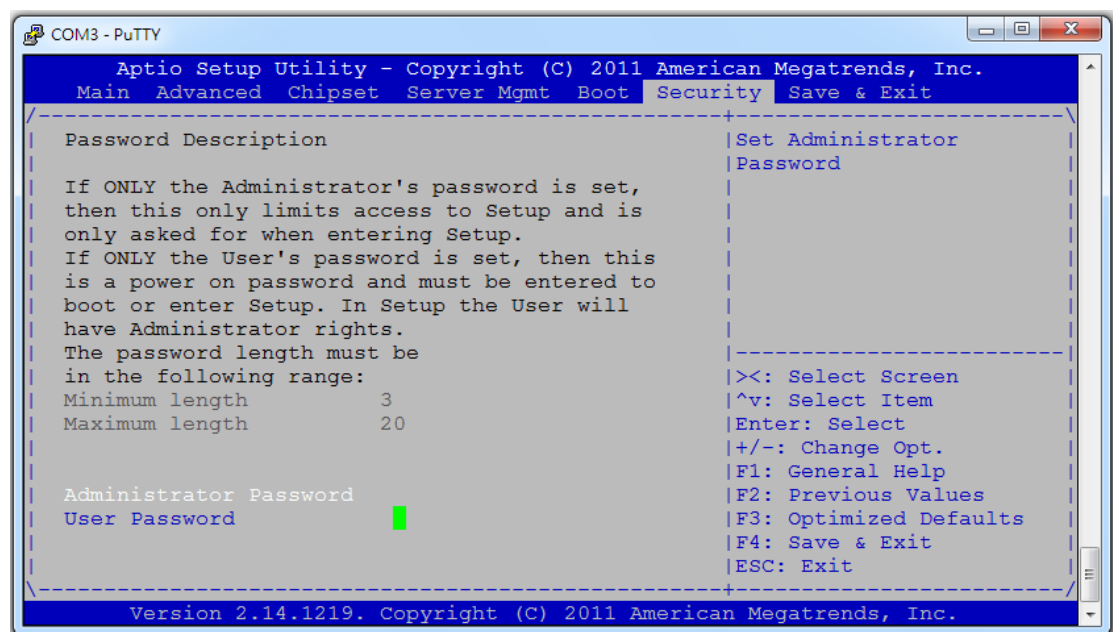


Figure 5.21 Security Configuration



Note:

- ◆ If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup.
- ◆ If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights.
- ◆ The password length must be in the following range:
 - Minimum length: 3
 - Maximum length: 20

5.9 Save & Exit Option

The MIC-5332 BIOS allows users to store BIOS configuration results as “User Defaults.” Users can select “Save as User Defaults” to record all changes which had been made in previous pages as the default setting for further use.

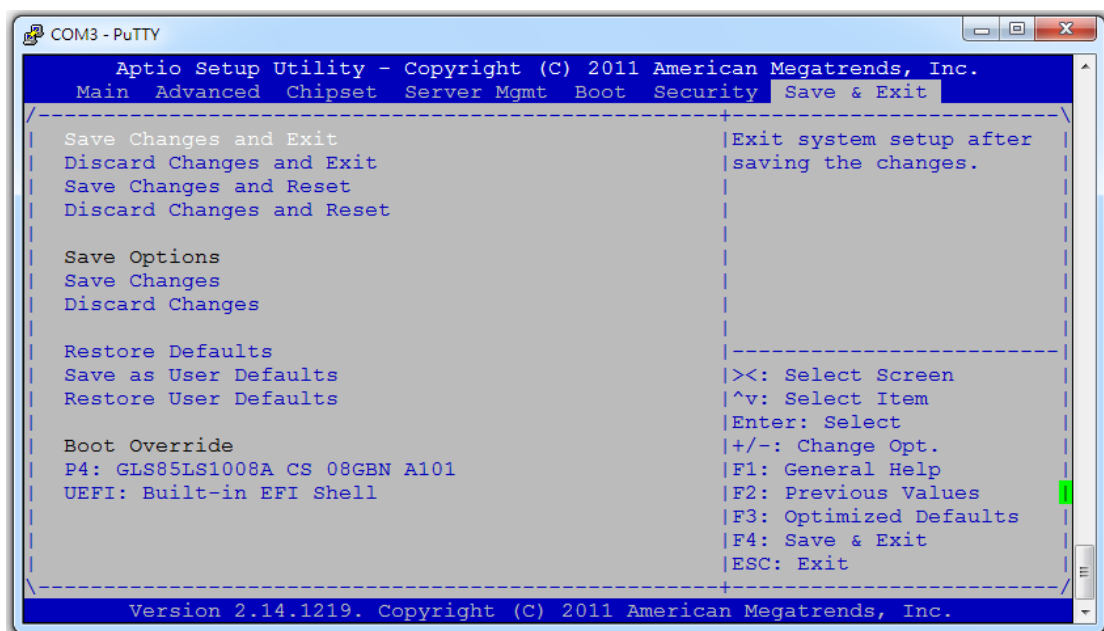


Figure 5.22 Save & Exit Configuration

Feature	Description
Save Changes and Exit	Exit system setup after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Save Changes and Reset	Reset system setup after saving the changes.
Discard Changes and Reset	Reset system setup without saving any changes.
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.

Restore Defaults	Restore/Load Default values for all the setup options.
Save as User Defaults	Save the changes done so far as User Defaults.
Restores User Defaults	Restore the User Defaults to all the setup options.

Table 5.14 Save & Exit Configuration

Chapter 6

Firmware Upgrade

This chapter describes how to update the IPMC FW, FPGA and BIOS for the MIC-5332.

6.1 HPM.1 Upgrade Functionality

All firmware updates/upgrades (IPMC firmware, FPGA configuration and BIOS SPI Flash) can be performed through HPM.1 over IPMI. Please follow the procedures described in the following sections.

6.2 IPMItool

Before upgrading, users need to prepare an update utility called “IPMItool” or any other HPM.1 compliant upgrade agent. For simplicity, the remaining descriptions reference IPMITool.

HPM.1 provides a way to upgrade firmware via different interfaces on ATCA platforms:

- LAN interface (RMCP),
- KCS (on-board payload interface – OS support needed), or
- IPMB (bridged via the Shelf Manager).

The following upgrade processes use KCS as interface over which upgrades are delivered to the IPMC. Using LAN or IPMB is similar, only the interface parameter in the related IPM command / IPMI tool needs to be adjusted accordingly.

6.3 BMC Upgrade

6.3.1 Upload the new BMC image

Type IPMItool HPM.1 upgrade command and select the new IPMC firmware image.

```
[root@localhost ~]#ipmitool hpm upgrade mic5332_standard_hpm_fw_00_46.img
```

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK

Performing preparation stage...

Target Product ID : 21298

Target Manufacturer ID: 10297

OK

Performing upgrade stage:

```
-----  
|ID | Name      | Versions          | Upload Progress | Upload| Image | | | | |
|  |           | Active| Backup| File | 0%      50%    100%| Time  | Size  |  
|---|-----|-----|-----|-----| |----+---+---+---| |-----|-----|  
| 1 | "Id" IPMC | 0.45 | 0.44 | 0.46 | |.....| | 00.51 | 4bf31 |  
-----
```

Firmware upgrade procedure successful

6.3.2 Activate HPM FW image

Although the new IPMC FW is successfully downloaded to the board (called “deferred” version), it needs to be activated before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# ipmitool hpm activate
```

```
PICMG HPM.1 Upgrade Agent 1.0.2:
```

```
Waiting firmware activation...OK
```

During the FW update the front panel FRU LED's 1 and 2 (red OOS and green payload LED) are flashing! This procedure needs around 30 seconds to finalize the update. It will need an IPMC reset to complete the FW upgrade.

The user can detect an upgrade failure **with an Integrity sensor event**.

6.4 FPGA Upgrade

6.4.1 Upload new FPGA image

Type IPMITool HPM.1 upgrade command and select the new IPMC firmware image.

```
[root@localhost ~]#ipmitool hpm upgrade mic5332_standard_hpm_fpga_02_14.img
PICMG HPM.1 Upgrade Agent 1.0.2:
```

Validating firmware image integrity...OK

Performing preparation stage...

Target Product ID : 21298

Target Manufacturer ID: 10297

OK

Performing upgrade stage:

ID	Name	Versions			Upload Progress			Upload	Image
		Active	Backup	File	0%	50%	100%	Time	Size
---	-----	-----	-----	-----		----+	----+	----+	
*2	5332 FPGA	2.13	2.12	2.14				01.08	6eea0

(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful

6.4.2 Activate HPM FPGA image

Although the new FPGA is successfully downloaded to the board (called “deferred” version), it needs to be activated before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# $ ipmitool hpm activate
PICMG HPM.1 Upgrade Agent 1.0.2:
```

6.4.3 Payload Reset

In order to activate the new FPGA image a payload reset is required.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed through different ways.

If the user is working on the OS via KCS a linux “reboot”, “poweroff” or “halt” will activate the new FPGA image.

If the user accesses the BMC through other interfaces (LAN/IPMB) a deactivation and activation cycle is needed, in order to update the FPGA.

During the FPGA update the front panel FRU LED's 1 and 2 (red OOS and green payload LED) are flashing! This procedure needs around 60 seconds to finalize the update.

6.4.4 Verify successful Upgrade

To verify the update process the hpm check of the IPMITool can be used again. Now the FPGA Backup Version should be the former active version, and the active version should be the version of the upload file.

```
[root@localhost ~]# ipmitool hpm check
```

```
PICMG HPM.1 Upgrade Agent 1.0.2:
```

```
-----Target Information-----
```

```
Device Id           : 0x22
Device Revision     : 0x81
Product Id          : 0x5332
Manufacturer Id     : 0x2839 (Advantech)
```

```
-----
```

ID	Name	Active	Backup
----	------	--------	--------

```
-----
```

0	5332 BL	0.45	--.---
1	5332 IPMC	0.45	0.45
*2	5332 FPGA	2.14	2.13
*3	5332 BIOS	0.23	0.23
*4	5332 NVRAM	0.04	--.---

```
-----
```

```
(*) Component requires Payload Cold Reset
```

6.5 BIOS Upgrade

6.5.1 Upload new BIOS image

Type IPMITool HPM.1 upgrade command and select the new BIOS image.

```
[root@localhost ~]# ipmitool hpm upgrade mic5332_standard_hpm_bios_00_23.img

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
    Target Product ID      : 21298
    Target Manufacturer ID: 10297
OK

Performing upgrade stage:

-----
|ID | Name      |      Versions          |      Upload Progress  | Upload| Image | | | | |
|  |           | Active| Backup| File | 0%      50%      100%| Time  | Size  |
|---|-----|-----|-----|-----| |-----+-----+-----| |-----|-----|
|*3 |"Id" BIOS |  0.21 |  0.21 |  0.23 | |.....| | 17.43 | 7c000c|
-----

(*) Component requires Payload Cold Reset

Firmware upgrade procedure successful
```

6.5.2 Activate HPM BIOS image

Although the new FPGA is successfully downloaded to the board (called “deferred” version), it needs to be activated before it will be functional. Use following HPM.1 command:

```
[root@localhost ~]# $ ipmitool hpm activate  
PICMG HPM.1 Upgrade Agent 1.0.2:
```

6.5.3 Payload Reset

In order to activate the new BIOS image a payload reset is required.

```
(*) Component requires Payload Cold Reset
```

The payload reset can be performed through different ways.

If the user is working on the OS via KCS a linux “reboot”, “poweroff” or “halt” will activate the new BIOS image.

If the user accesses the BMC through other interfaces (LAN/IPMB) a deactivation and activation cycle is needed, in order to update the FPGA.

6.5.4 Verify successful Upgrade

To verify the update process the hpm check of the IPMItool can be used again.

Now the BIOS Backup Version should be the former active version, and the active version should be the version of the upload file.

```
[root@localhost ~]# ipmitool hpm check
```

```
PICMG HPM.1 Upgrade Agent 1.0.2:
```

```
-----Target Information-----
```

```
Device Id           : 0x22
Device Revision     : 0x81
Product Id          : 0x5332
Manufacturer Id     : 0x2839 (Advantech)
```

```
-----
|ID | Name      | Versions |
|   |           | Active| Backup|
-----
```

6.6 NVRAM Upgrade

In contrast to the BIOS image update, the setting update image is not directly written to any of the BIOS SPI flashes. The BIOS settings are stored in the external SPI flash of the IPMC to support a deferred activation. For extended flexibility the external SPI flash supports different sections to store up to four BIOS setting images in the external flash at the same time. Each of these settings can be set to “active” at any time and will be copied to the active BIOS flash at the next OS boot.

6.6.1 Select Upgrade Section (optional)

As described above, the IPMC provides multiple upgrade sections for different NVRAM sections. OEM commands are used to select the upload and activation setting from the different BIOS setting sections in the external flash.

```
[root@localhost ~]# ipmitool raw 0x2E 0x40 0x39 0x28 0x00 0x03 0x01  
<section>
```

6.6.2 Upload new NVRAM image

Type IPMITool HPM.1 upgrade command and select the new NVRAM image.

```
[root@localhost ~]# ipmitool hpm upgrade mic5332_standard_hpm_bios_00_05.img
PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...
    Target Product ID      : 21298
    Target Manufacturer ID: 10297
OK

Performing upgrade stage:

-----
|ID | Name      |      Versions          |      Upload Progress  | Upload| Image | | |
|  |           | Active| Backup| File | 0%      50%      100%| Time  | Size  |
|---|-----|-----|-----|-----|-----+-----+-----|-----|-----|
```

6.6.3 Activate HPM NVRAM image

Since there exist more than one possible NVRAM sections, an OEM command is used to activate a selected NVRAM section.

```
[root@localhost ~]# ipmitool raw 0x2E 0x40 0x39 0x28 0x00 0x03 0x02 <section>
```

6.6.4 Payload Reset

In order to activate the new NVRAM image a payload reset is required.

(*) Component requires Payload Cold Reset

The payload reset can be performed through different ways.

If the user is working on the OS via KCS a linux “reboot”, “poweroff” or “halt” will activate the new NVRAM image.

If the user accesses the BMC through other interfaces (LAN/IPMB) a deactivation and activation cycle is needed, in order to update the NVRAM.

Appendix A

IPMI/PICMG Command Subset Supported by IPMC

IPM Device “Global” Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Get Device ID	20.1	App	01h	Mandatory
Cold Reset	20.2	App	02h	Optional
Warm Reset	20.3	App	03h	Optional
Get Self Test Results	20.4	App	04h	Mandatory
Get Device GUID	20.8	App	08h	Optional
Broadcast “Get Device ID	20.9	App	01h	Mandatory

BMC Watchdog Timer Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Reset Watchdog Timer	27.5	App	22h	Mandatory
Set Watchdog Timer	27.6	App	24h	Mandatory
Get Watchdog Timer	27.7	App	25h	Mandatory

BMC Device and Messaging Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Set BMC Global Enables	22.1	App	2Eh	Optional/Mandatory
Get BMC Global Enables	22.2	App	2Fh	Optional/Mandatory
Clear Message Flags	22.3	App	30h	Optional/Mandatory
Get Message Flags	22.4	App	31h	Optional/Mandatory
Get Message	22.6	App	33h	Optional/Mandatory
Send Message	22.7	App	34h	Optional/Mandatory
Get System GUID	22.14	App	37h	Optional
Get Channel Authentication Capabilities	22.13	App	38h	Optional
Get Session Challenge	22.15	App	39h	Optional
Activate Session	22.17	App	3Ah	Optional
Set Session Privilege Level	22.18	App	3Bh	Optional
Close Session	22.19	App	3Ch	Optional
Get Session Info	22.20	App	3Dh	Optional
Set Channel Access	22.22	App	40h	Optional
Get Channel Access	22.23	App	41h	Optional
Get Channel Info	22.24	App	42h	Optional

Set User Access	22.26	App	43h	Optional
Get User Access	22.27	App	44h	Optional
Set User Name	22.28	App	45h	Optional
Get User Name	22.29	App	46h	Optional
Set User Password	22.30	App	47h	Optional
Activate Payload	24.1	App	48h	None
Deactivate Payload	24.2	App	49h	None
Set User Payload Access	24.6	App	4Ch	None
Get User Payload Access	24.7	App	4Dh	None
Get Channel Payload Support	24.8	App	4Eh	None
Get Channel Payload Version	24.9	App	4Fh	None
Master Write-Read	22.11	App	52h	Optional/Mandatory
Get Channel Cipher Suites	22.15	App	54h	None
Set Channel Security Keys	22.25	App	56h	None

Event Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Set Event Receiver	29.1	S/E	00h	Mandatory
Get Event Receiver	29.2	S/E	01h	Mandatory
Platform Event (a.k.a. "Event Message")	23.3	S/E	02h	Mandatory

Sensor Device Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Get Device SDR Info	35.2	S/E	20h	Mandatory
Get Device SDR	35.3	S/E	21h	Mandatory
Reserve Device SDR Repository	35.4	S/E	22h	Mandatory
Get Sensor Reading Factors	35.5	S/E	23h	Optional
Set Sensor Hysteresis	35.6	S/E	24h	Optional
Get Sensor Hysteresis	35.7	S/E	25h	Optional
Set Sensor Threshold	35.8	S/E	26h	Optional
Get Sensor Threshold	35.9	S/E	27h	Optional
Set Sensor Event Enable	35.10	S/E	28h	Optional
Get Sensor Event Enable	35.11	S/E	29h	Optional
Get Sensor Event Status	35.13	S/E	2Bh	Optional

Get Sensor Reading	35.14	S/E	2Dh	Mandatory
Get Sensor Type	35.16	S/E	2Fh	Optional

FRU Device Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Get FRU Inventory Area Info	34.1	Storage	10h	Mandatory
Read FRU Data	34.2	Storage	11h	Mandatory
Write FRU Data	34.3	Storage	12h	Mandatory

SEL Device Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Get SEL Info	31.2	Storage	40h	Mandatory
Reserve SEL	31.4	Storage	42h	Optional
Get SEL Entry	31.5	Storage	43h	Mandatory
Add SEL Entry	31.6	Storage	44h	Mandatory
Clear SEL	31.9	Storage	47h	Mandatory
Get SEL Time	31.10	Storage	48h	Mandatory
Set SEL Time	31.11	Storage	49h	Mandatory

LAN Device Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Set LAN Configuration Parameters	23.1	Transport	01h	Optional/Mandatory
Get LAN Configuration Parameters	23.2	Transport	02h	Optional/Mandatory

Serial/Modem Device Commands

Command	IPMI Spec Ref	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Set Serial/Modem Configuration	25.1	Transport	10h	Optional/Mandatory
Get Serial/Modem Configuration	25.2	Transport	11h	Optional/Mandatory
Set SOL Configuration Parameters	26.2	Transport	21h	None
Get SOL Configuration Parameters	26.3	Transport	22h	None

AdvancedTCA® Commands

Command	PICMG® 3.0 Table	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Get PICMG Properties	3-11	PICMG	00h	Mandatory
Get Address Info	3-10	PICMG	01h	Mandatory
FRU Control	3-27	PICMG	04h	Mandatory
Get FRU LED Properties	3-29	PICMG	05h	Mandatory
Get LED Color Capabilities	3-30	PICMG	06h	Mandatory
Set FRU LED State	3-31	PICMG	07h	Mandatory
Get FRU LED State	3-32	PICMG	08h	Mandatory
Set IPMB State	3-70	PICMG	09h	Mandatory
Set FRU Activation Policy	3-20	PICMG	0Ah	Mandatory
Get FRU Activation Policy	3-21	PICMG	0Bh	Mandatory
Set FRU Activation	3-19	PICMG	0Ch	Mandatory
Get Device Locator Record ID	3-39	PICMG	0Dh	Mandatory
Set Port State	3-59	PICMG	0Eh	Optional/Mandatory
Get Port State	3-60	PICMG	0Fh	Optional/Mandatory
Compute Power Properties	3-82	PICMG	10h	Mandatory
Set Power Level	3-84	PICMG	11h	Mandatory
Get Power Level	3-83	PICMG	12h	Mandatory
Get IPMB Link Info	3-68	PICMG	18h	Optional/Mandatory
FRU Control Capabilities	3-26	PICMG	1Eh	Mandatory

HPM.1 Upgrade Commands

Command	HPM.1 Table	NetFn	CMD	IPMI / PICMG3.0 / AMC2.0 Requirement
Get target upgrade capabilities	3-3	PICMG	2Eh	Mandatory
Get component properties	3-5	PICMG	2Fh	Mandatory
Abort Firmware Upgrade	3-15	PICMG	30h	Optional
Initiate upgrade action	3-8	PICMG	31h	Mandatory
Upload firmware block	3-9	PICMG	32h	Mandatory
Finish firmware upload	3-10	PICMG	33h	Mandatory
Get upgrade status	3-2	PICMG	34h	Optional/Mandatory
Activate firmware	3-11	PICMG	35h	Mandatory
Query Self-test Results	3-12	PICMG	36h	Optional/Mandatory
Query Rollback status	3-13	PICMG	37h	Optional/Mandatory
Initiate Manual Rollback	3-14	PICMG	38h	Optional/Mandatory

Advantech OEM commands

Advantech management solutions support extended OEM IPMI command sets, based on the IPMI defined OEM/Group Network Function (NetFn) Codes 2Eh, 2Fh.

The first three data bytes of IPMI requests and responses under the OEM/Group Network Function explicitly identify the OEM vendor that specifies the command functionality. To be more precise, the vendor IANA Enterprise Number for the defining body occupies the first three data bytes in a request, and the first three data bytes following the completion code position in a response. Advantech's IANA Enterprise Number used for OEM commands is 002839h.

The BMC supports Advantech IPMI OEM commands listed in below table.

Command	LUN	NetFn	CMD
Store Configuration Settings	00h	2Eh, 2Fh	40h
Read Configuration Settings	00h	2Eh, 2Fh	41h
Read Port 80 (BIOS POST Code)	00h	2Eh, 2Fh	80h
Clear CMOS	00h	2Eh, 2Fh	81h
Read MAC Address	00h	2Eh, 2Fh	E2h
Load Default Configuration	00h	2Eh, 2Fh	F2h

A.1 IPMITool raw command

To be able to use the Advantech OEM commands with the open source IPMITool, users have to employ the “raw” command of IPMITool. Please find below command structure details of the IPMITool raw command.

General raw request:

```
ipmitool raw <netfn> <cmd> [data]
```

Response, if raw <netfn> is 2Eh (OEM/Group):

```
<IANA Enterprise Number> [data]
```

A.2 Configuration Setting OEM commands

The Read and Store Configuration OEM commands can be used to read and change several important board settings. The following sub-chapters describe the needed command details.

A.2.1 LAN controller interface selection

The MMC firmware provides an OEM IPMI command to allow users to switch the MMC connected NC-SI interface between one front panel LAN IO RJ-45 connector and the Base interface. These commands can be used to read out the actual selected IPMI-over-LAN / Serial-over-LAN interface and to change the selection.

LAN controller interface selection settings:

00h: Front panel LAN IO

01h: Base Interface LAN BI (default)

Read LAN Interface selection:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x00
```

Response:

```
39 28 00 <setting>
```

Change LAN Interface selection:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x00 <setting>
```

Response:

```
39 28 00
```

A.2.2 LAN controller channel selection and priority

In addition to the selected LAN controller interface, users may need to configure each single LAN controller channel (port) as dedicated NC-SI interface to the BMC.

Additional OEM commands for the configuration of the NC-SI LAN controller channel selection and priority are provided to allow a flexible configuration.

LAN channel selection priority setting list:

- 0 = The first channel that links up, gets the NC-SI connection to the BMC.
- 1 = Channel 1 is the preferred port if it is up, otherwise use channel 2 if it is up.
- 2 = Channel 2 is the preferred port if it is up, otherwise use channel 1 if it is up.
- 3 = Channel 1 is the only allowed port, always use it, never change to channel 2.

4 = Channel 2 is the only allowed port, always use it, never change to channel 1.

The NC-SI LAN controller channel setting will be stored permanently (non-volatile EEPROM). The default value is 0.

Read LAN channel selection priority:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x04 0x01
```

Response:

```
39 28 00 <setting>
```

Change LAN channel selection priority:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x04 0x01 <setting>
```

Response:

```
39 28 00
```

A.2.3 FPGA COM port UART MUX

MIC-5332 implements several serial interfaces, which can be configured in some ways. This is done inside the FPGA with the help of an UART MUX (refer to chapter [<x.x.x – UART MUX>](#)). The BMC provides OEM commands to configure these UARTs via IPMI. Following COM1 / COM2 port settings are available (Caution: Verify note below about the UART dependency!):

COM interfaces:

Port	Interface
0x00	COM1
0x01	COM2

Table 1: COM interfaces

COM1 MUX:

Setting	Connection
0x00	no interface connected, open
0x01	Serial-over-LAN (SOL)

0x02	Front Panel RJ45
0x03	Front panel mini-USB (default)
0x04	RTM mini-USB
0x05	RTM RJ45
0x0F	Automatic mode

Table 2: COM1 UART MUX settings

COM2 MUX:

Setting	Connection
0x00	no interface connected, open
0x01	Serial-over-LAN (SOL)
0x02	Front Panel RJ45
0x03	Front panel mini-USB (default)
0x04	RTM mini-USB
0x05	RTM RJ45

Table 3: COM2 UART MUX settings

Important Note: The COM1 UART is the main interface with higher priority! There is an important dependency between COM1 and COM2 UARTs, users should know and aware of:

The COM2 MUX can ONLY be used, if the COM1 MUX is set to SOL (0x01)! If the COM1 MUX has any other settings than SOL, COM2 is permanently fixed to SOL and the COM2 MUX OEM command setting is ignored.

Read COM port UART MUX setting:

```
ipmitool raw 0x2e 0x41 0x39 0x28 0x00 0x08 <port>
```

Response:

```
39 28 00 <setting>
```

Change COM port UART MUX setting:

```
ipmitool raw 0x2e 0x40 0x39 0x28 0x00 0x08 <port> <setting>
```

Response:

```
39 28 00
```

A.3 Read Port 80 (BIOS POST Code) OEM command

To be able to read out the actual BIOS boot state via IPMI, the MMC provides an Advantech OEM command to reflect the actual BIOS POST (Port 80) code.

```
ipmitool raw 0x2e 0x80 0x39 0x28 0x00
```

Response:

```
39 28 00 <POST Code>
```

A.4 Load NVRAM defaults OEM command

The BMC implements an OEM command to be able to load the NVRAM defaults from SW side without the need of extracting the blade and performing any jumper plug and re-plug.

```
ipmitool raw 0x2e 0x81 0x39 0x28 0x00
```

Response:

```
39 28 00
```

A.5 MAC Address Mirroring OEM command

The blade LAN Controller MAC addresses will also be stored in the FRU EEPROM, making the MAC's available even if the payload is not powered.

The MIC-5332 board is equipped with 7 MAC addresses in total. Please find below the used order in the FRU EEPROM Internal Use Area:

MAC Number	LAN Interface
0	Fabric interface 1
1	Fabric interface 2
2	Base Interface 1
3	Base Interface 2
4	IO Interface 1
5	IO Interface 2

6	PCH MAC
7	IPMC MAC
8..x	FMM MAC addresses (if plugged)

Table 4: MAC Address mapping table

Read MAC Address OEM command:

```
ipmitool raw 0x2e 0xe2 0x39 0x28 0x00 <MAC Number>
```

Response:

```
39 28 00 <MAC-Address>
```

A.6 Load Default Configuration OEM command

Several configurations settings are provided by the IPMC (verify chapter [<x.x.x Configuration Setting OEM commands>](#)). To reset all of them to their default values, a single OEM command is available to perform this with only one IPMI command.

```
ipmitool raw 0x2e 0xF2 0x39 0x28 0x00
```

Response:

```
39 28 00
```

Appendix B

Zone 1 P10 Pin-out

Pin	pin name	Pin use
1	Reserved	No connected
2	Reserved	No connected
3	Reserved	No connected
4	Reserved	No connected
5	HA0	Hardware Address bit 0
6	HA1	Hardware Address bit 1
7	HA2	Hardware Address bit 2
8	HA3	Hardware Address bit 3
9	HA4	Hardware Address bit 4
10	HA5	Hardware Address bit 5
11	HA6	Hardware Address bit 6
12	HA7/P	Hardware Address bit 7
13	SCL_A	IPMB0-A clock
14	SDA_A	IPMB0-A data
15	SCL_B	IPMB0-B clock
16	SDA_B	IPMB0-B data
17	MT1_TIP	No connected
18	MT2_TIP	No connected
19	RING_A	No connected
20	RING_B	No connected
21	MT1_RING	No connected
22	MT2_RING	No connected
23	RRTN_A	No connected
24	RRTN_B-	No connected
25	SHELF_GND	Connect to shelf ground
26	LOGIC_GND	Connect to logic ground
27	ENABLE_B	Enable -48V_B power
28	VRTN_A	-48V return voltage VRTN_A input
29	VRTN_B	-48V return voltage VRTN_B input
30	-48V_EARLY_A	-48V pre-charge input for -48V_A
31	-48V_EARLY_B	-48V pre-charge input for -48V_B
32	ENABLE_A	Enable -48V_A power

33	-48V_A	-48V input feed A
34	-48V_B	-48V input feed B

Appendix C

Zone 2 Interface pin-out

Zone 2 J20 pin out – Update Channel

[illegible]

Zone 2 J22 pin out – Base Interface and Fabric Interface

J22	Pin							
Row	A	B	C	D	E	F	G	H
1	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
2	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
3	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
4	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
5	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
6	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
7	FI_CH4 Tx2+	FI_CH4 Tx2-	FI_CH4 Rx2+	FI_CH4 Rx2-	FI_CH4 Tx3+	FI_CH4 Tx3-	FI_CH4 Rx3+	FI_CH4 Rx3-
8	FI_CH4 Tx0+	FI_CH4 Tx0-	FI_CH4 Rx0+	FI_CH4 Rx0-	FI_CH4 Tx1+	FI_CH4 Tx1-	FI_CH4 Rx1+	FI_CH4 Rx1-
9	FI_CH3 Tx2+	FI_CH3 Tx2-	FI_CH3 Rx2+	FI_CH3 Rx2-	FI_CH3 Tx3+	FI_CH3 Tx3-	FI_CH3 Rx3+	FI_CH3 Rx3-
10	FI_CH3 Tx0+	FI_CH3 Tx0-	FI_CH3 Rx0	FI_CH3 Rx0-	FI_CH3 Tx1+	FI_CH3 Tx1-	FI_CH3 Rx1+	FI_CH3 Rx1-

Zone 2 J23 pin out – Base Interface and Fabric Interface

[illegible]

Appendix D

Zone 3 Interface (RTM) pin-out

Zone 3 J31 pin out

J31	Pin							
Row	M							A
8	RTM_+12V				RTM_3.3V_MP		RTM_IPMBL	
7	RTM_MMC_	RTM_PERST0#	RTM_ENABLE#	RTM_PS#	RTM_LINK			
6	not connected		not connected		RTM_USB1		RTM_USB0	
5	not connected				not connected			
4	RTM_UART1				RTM_UART0			
3	not connected		RTM_PCIE2_CLK		RTM_PCIE1_CLK		RTM_PCIE0_CLK	
2	PEx4_2: RTM_PE4-0_3				PEx4_2: RTM_PE4-0_2			
1	PEx4_2: RTM_PE4-0_1				PEx4_2: RTM_PE4-0_0			

Zone 3 J32 pin out

J32	Pin							
Row	M							A
8	not connected		not connected		RTM_USB3		RTM_USB2	
7	TCLKD		TCLKC		TCLKB		TCLKA	
6	not connected				not connected			
5	not connected				not connected			
4	not connected				not connected			
3	SATA1: RTM_SATA1				SATA1: RTM_SATA0			
2	SAS0: RTM_SAS3				SAS0: RTM_SAS2			
1	SAS0: RTM_SAS1				SAS0: RTM_SAS0			

Zone 3 J34 pin out

J34	Pin							
Row	M							A
8	PEx16_1: RTM_PE16-1_0 RX		PEx16_1: RTM_PE16-1_4 RX		PEx16_1: RTM_PE16-1_0 TX		PEx16_1: RTM_PE16-1_4 TX	
7	PEx16_1: RTM_PE16-1_0 RX		PEx16_1: RTM_PE16-1_12 RX		PEx16_1: RTM_PE16-1_8 TX		PEx16_1: RTM_PE16-1_12 TX	
6	PEx16_1: RTM_PE16-1_1 RX		PEx16_1: RTM_PE16-1_5 RX		PEx16_1: RTM_PE16-1_1 TX		PEx16_1: RTM_PE16-1_5 TX	
5	PEx16_1: RTM_PE16-1_2 RX		PEx16_1: RTM_PE16-1_13 RX		PEx16_1: RTM_PE16-1_9 TX		PEx16_1: RTM_PE16-1_13 TX	
4	PEx16_1: RTM_PE16-1_2 RX		PEx16_1: RTM_PE16-1_6 RX		PEx16_1: RTM_PE16-1_2 TX		PEx16_1: RTM_PE16-1_6 TX	

3	PEx16_1: RTM_PE16-1_10 RX	PEx16_1: RTM_PE16-1_14 RX	PEx16_1: RTM_PE16-1_10 TX	PEx16_1: RTM_PE16-1_14 TX
2	PEx16_1: RTM_PE16-1_3 RX	PEx16_1: RTM_PE16-1_7 RX	PEx16_1: RTM_PE16-1_3 TX	PEx16_1: RTM_PE16-1_7 TX
1	PEx16_1: RTM_PE16-1_11 RX	PEx16_1: RTM_PE16-1_15 RX	PEx16_1: RTM_PE16-1_11 TX	PEx16_1: RTM_PE16-1_15 TX

Appendix E

FMM Interface pin-out

	F	E	D	C	B	A
1	NC	GND	FM_PRSENT#	GND	NC	GND
2	GND	NC	GND	FI3_RX0_P	GND	PCIE1_TX0_P
3	GND	NC	GND	FI3_RX0_N	GND	PCIE1_TX0_N
4	NC	GND	FI3_RX1_P	GND	PCIE1_TX1_P	GND
5	NC	GND	FI3_RX1_N	GND	PCIE1_TX1_N	GND
6	GND	NC	GND	FI3_RX2_P	GND	PCIE1_TX2_P
7	GND	NC	GND	FI3_RX2_N	GND	PCIE1_TX2_N
8	NC	GND	FI3_RX3_P	GND	PCIE1_TX3_P	GND
9	NC	GND	FI3_RX3_N	GND	PCIE1_TX3_N	GND
10	GND	NC	GND	FI4_RX0_P	GND	PCIE1_TX4_P
11	GND	NC	GND	FI4_RX0_N	GND	PCIE1_TX4_N
12	NC	GND	FI4_RX1_P	GND	PCIE1_TX5_P	GND
13	NC	GND	FI4_RX1_N	GND	PCIE1_TX5_N	GND
14	GND	NC	GND	FI4_RX2_P	GND	PCIE1_TX6_P
15	GND	NC	GND	FI4_RX2_N	GND	PCIE1_TX6_N
16	NC	GND	FI4_RX3_P	GND	PCIE1_TX7_P	GND
17	NC	GND	FI4_RX3_N	GND	PCIE1_TX7_N	GND
18	GND	NC	GND	PCIE0_RX0_P	GND	PCIE1_RX0_P
19	GND	NC	GND	PCIE0_RX0_N	GND	PCIE1_RX0_N
20	NC	GND	PCIE0_RX1_P	GND	PCIE1_RX1_P	GND
21	NC	GND	PCIE0_RX1_N	GND	PCIE1_RX1_N	GND
22	GND	NC	GND	PCIE0_RX2_P	GND	PCIE1_RX2_P
23	GND	NC	GND	PCIE0_RX2_N	GND	PCIE1_RX2_N
24	NC	GND	PCIE0_RX3_P	GND	PCIE1_RX3_P	GND
25	NC	GND	PCIE0_RX3_N	GND	PCIE1_RX3_N	GND
26	GND	NC	GND	PCIE0_RX4_P	GND	PCIE1_RX4_P
27	GND	NC	GND	PCIE0_RX4_N	GND	PCIE1_RX4_N
28	FPGA_GPIO_P3	GND	PCIE0_RX5_P	GND	PCIE1_RX5_P	GND
29	FPGA_GPIO_N3	GND	PCIE0_RX5_N	GND	PCIE1_RX5_N	GND
30	GND	FPGA_GPIO_P5	GND	PCIE0_RX6_P	GND	PCIE1_RX6_P
31	GND	FPGA_GPIO_N5	GND	PCIE0_RX6_N	GND	PCIE1_RX6_N
32	FPGA_GPIO_P7	GND	PCIE0_RX7_P	GND	PCIE1_RX7_P	GND

33	FPGA_GPIO_N7	GND	PCIE0_RX7_N	GND	PCIE1_RX7_N	GND
34	GND	NC	GND	PCIE0_REF_CLK_P	GND	PCIE1_REF_CLK_P
35	GND	NC	GND	PCIE0_REF_CLK_P	GND	PCIE1_REF_CLK_P
36	NC	GND	#FI3_LED_HS	GND	SAS_SATA0_TX_P	GND
37	NC	GND	#FI3_LED_LS	RST#	SAS_SATA0_TX_N	SAS_SATA0_RX_P
38	GND	NC	3.3V_SB	I2C_SCL	GND	SAS_SATA0_RX_N
39	12V	NC	JTAG_EN#	I2C_SDA	NC	GND
40	12V	GND	GA1	GA0	NC	NC
	HPC only		LPC		HPC only	

	K	J	H	G
1	NC	GND	PGD	GND
2	GND	NC	GND	FI3_TX0_P
3	GND	NC	GND	FI3_TX0_N
4	NC	GND	FI3_TX1_P	GND
5	NC	GND	FI3_TX1_N	GND
6	GND	NC	GND	FI3_TX2_P
7	GND	NC	GND	FI3_TX2_N
8	NC	GND	FI3_TX3_P	GND
9	NC	GND	FI3_TX3_N	GND
10	GND	NC	GND	FI4_TX0_P
11	GND	NC	GND	FI4_TX0_N
12	NC	GND	FI4_TX1_P	GND
13	NC	GND	FI4_TX1_N	GND
14	GND	NC	GND	FI4_TX2_P
15	GND	NC	GND	FI4_TX2_N
16	NC	GND	FI4_TX3_P	GND
17	NC	GND	FI4_TX3_N	GND
18	GND	NC	GND	PCIE0_TX0_P
19	GND	NC	GND	PCIE0_TX0_N
20	NC	GND	PCIE0_TX1_P	GND
21	NC	GND	PCIE0_TX1_N	GND
22	GND	NC	GND	PCIE0_TX2_P
23	GND	NC	GND	PCIE0_TX2_N
24	NC	GND	PCIE0_TX3_P	GND
25	NC	GND	PCIE0_TX3_N	GND
26	GND	FPGA_GPIO_P0	GND	PCIE0_TX4_P

27	GND	FPGA_GPIO_N0	GND	PCIE0_TX4_N
28	FPGA_GPIO_P2	GND	PCIE0_TX5_P	GND
29	FPGA_GPIO_N2	GND	PCIE0_TX5_N	GND
30	GND	FPGA_GPIO_P4	GND	PCIE0_TX6_P
31	GND	FPGA_GPIO_N4	GND	PCIE0_TX6_N
32	FPGA_GPIO_P6	GND	PCIE0_TX7_P	GND
33	FPGA_GPIO_N6	GND	PCIE0_TX7_N	GND
34	GND	NC	GND	NC
35	GND	NC	GND	NC
36	NC	GND	NC	GND
37	NC	GND	NC	NC
38	GND	USB2_DP	GND	#FI4_LED_HS
39	USB1_DP	USB2_DN	12V	#FI4_LED_LS
40	USB1_DN	GND	12V	GND
	HPC only		LPC	